THE UNIVERSITY OF ALBERTA

CONSECUTIVE CONTROL OF CONVERTERS

BY

© ELWEYA M.F. RASHED (nee MOHANNA)

A THESIS

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled "Consecutive Control Of Converters" submitted by Mrs. Elweya M.F. Rashed (nee Mohanna) in partial fulfilment of the requirements for the degree of Master of Science.

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ABSTRACT

A new method for the control of phase-controlled converters is presented. Among the several features of this method, the two groups of valves of the converter are gated separately.

Analysis of the performance characteristics of the converter is carried out, and d.c. output voltage waveforms are obtained at different firing angles. The variation of harmonic components of the d.c. terminal voltage with the firing angle is also obtained.

A comparison between the conventional controls and the new one shows that the new control has many advantages over conventional controls. Mainly, the reduction of reactive loading of the a.c. side, and almost zero harmonic content at zero output voltage.

A test is carried out to check the performance of the control circuit. The circuit is proved to work satisfactorily for the rectification region. No results are obtained for the inversion region. However, it is believed that if the control circuit were tested with an active load, the performance will be the same as that obtained by theoretical analysis.

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LIST OF SYMBOLS

V_N	peak value of phase-to-neutral voltage at converter input.
$\hat{V}_N$	rms value of phase-to-neutral voltage at converter input.
V_d	mean value of voltage at d.c. terminals of phase-controlled converter, at firing angles α_1, α_2.
V_{dmax}	maximum possible mean value of voltage at d.c. terminals of phase-controlled converter at $\alpha_1=\alpha_2=0°$.
v_d	instantaneous value of voltage at d.c. terminals of phase-controlled converter.
$V_{AC(AB,...)}$	commutating voltage of valve 1,2,...
r	ratio of d.c. terminal voltage of converter at firing angles α_1, α_2 to maximum possible mean d.c. terminal voltage, obtained at $\alpha_1=\alpha_2=0°$.
I_{rms}	rms value of the converter input line current.
I_1	peak value of the fundamental component of the converter input line current.
$\hat{I}_1$	rms value of the fundamental component of the converter input line current.
I_P	peak value of the fundamental in-phase component of converter input current.

$\hat{I}_P$	rms value of the fundamental in-phase component of converter input current
I_Q	peak value of the fundamental quadrature component of converter input current
$\hat{I}_Q$	rms value of the fundamental quadrature component of converter input current
$i_{A(B,C)}$	instantaneous value of current in converter input line A(B,C)
I_d	direct current at output of phase-controlled converter
i_d	instantaneous value of current at d.c. terminals of phase-controlled converter
f_i	frequency of supply at input of converter
ω_i	$2\pi f_i$
θ_i	$2\pi f_i t$
f_H	harmonic frequency
α	converter firing angle
α_1	firing angle of the upper valves of a 6-pulse converter
α_2	firing angle of the lower valves of a 6-pulse converter
μ	commutation overlap angle
δ	thyristor extinction or recovery angle

CHAPTER I

INTRODUCTION

Since its introduction some ten years ago, the silicon-controlled rectifier, or thyristor, has become firmly established as the active power control element of static electrical power conversion equipments of many types, ranging in power ratings from a few hundred watts to several megawatts.

One particular type of static power conversion circuits which today employ thyristors, is the phase-controlled converter, which converts alternating current to direct current or vice versa.

The phase-controlled converter, of course, has been employed, using older types of grid-controlled rectifier, for many years prior to the introduction of the thyristor. Nonetheless, the emergence of the thyristor, in conjunction with the rapid technological advances that have been made in the area of transistors, integrated circuits, and solid state devices of all types, has given birth to a much wider field of applications for the phase-controlled converter. As a result, many innovations have been made, in terms of both circuitry and control concepts.

In the application of phase-controlled converters, there are two considerations. First, the principle used for controlling the phase of the thyristor firing pulses, and second, the mode of operation of the converter, i.e. whether it is operated as an inverter or as a rectifier.

Conventional methods of firing pulse timing control, together with techniques used in the operation of the phase controlled converters will be discussed briefly here.

The main objective of this work is to represent a detailed description and explanation of the fundamental principles of operation and control of a 3-phase controlled converter with a new control technique. Also this work will represent a practical control scheme to obtain the desired control performance.

CHAPTER II

PHASE-CONTROLLED CONVERTERS

OPERATION AND CONTROL

2.1 Operation Of Phase-Controlled Converters

The operation of phase-controlled converters will be discussed with reference to the 3-phase bridge configuration of Fig. 2.1(a).

With regular diodes the current transfer between two diodes starts as soon as the commutating voltage of the succeeding valve rises above that of the preceeding one. Each valve conducts during the portion of the cycle in which its anode voltage is the most positive. Thus the d.c. circuit is given the highest possible potential at any instant and the direct voltage is a maximum. This is illustrated in Fig. 2.1(b), at which the current transfers from valve 6 to valve 2 at the instant ωt_o at which V_{BC}, the commutating voltage for valve 2, rises higher than V_{AB}, the commutating voltage for valve 6, and so on. The valve numbers indicate their order of conduction.

If, however, the transition is delayed by a certain angle, α say, then the current is forced to flow in a valve which has lower positive average voltage during its conduction period. Thus the direct voltage is determined by a lower potential during a certain period of time, and the average value is reduced. This is illustrated in Fig. 2.1(c).

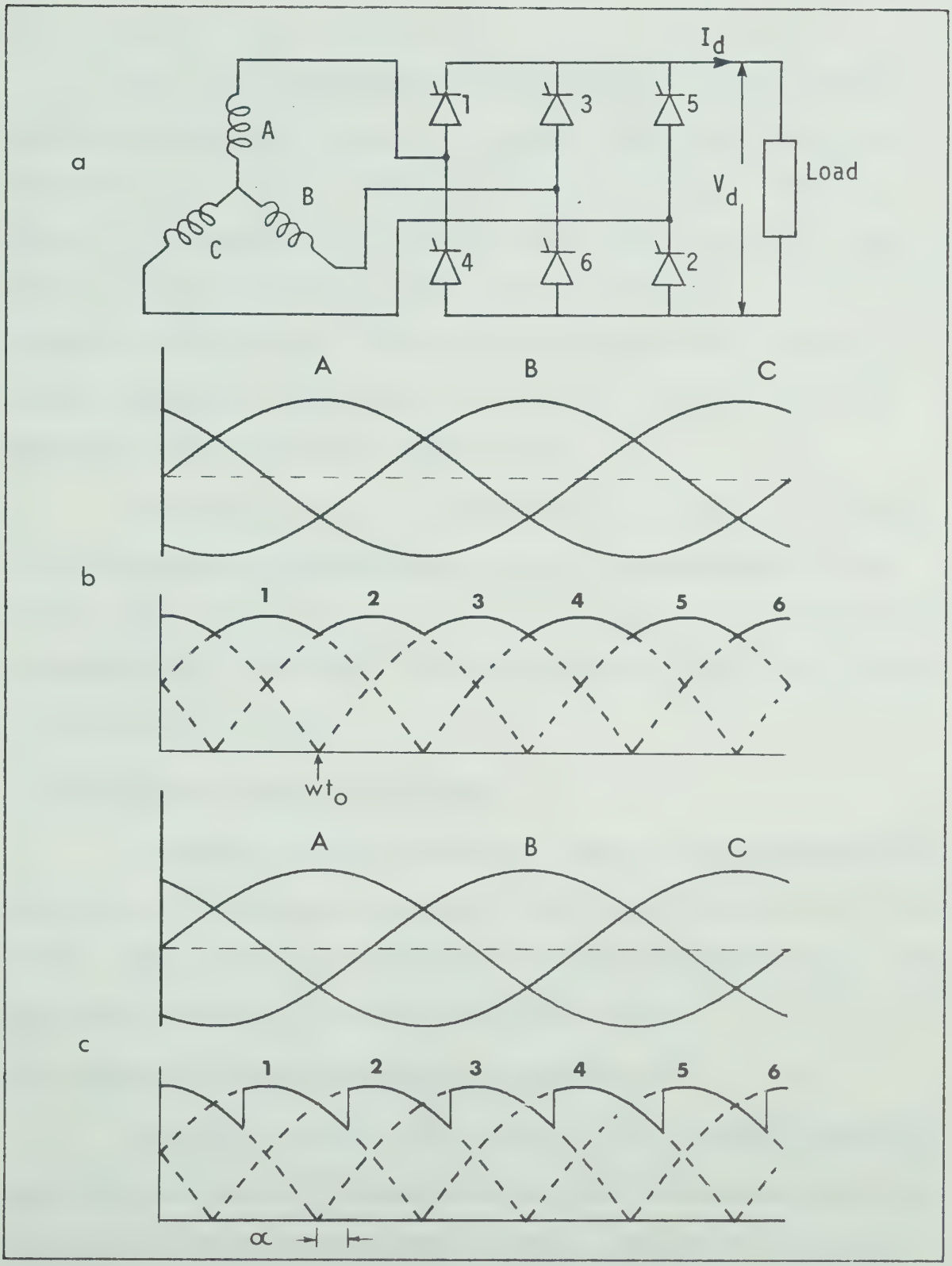


Fig. 2.1 (a) 3-phase bridge converter

(b) Output d.c. voltage without phase delay

(c) Output d.c. voltage with angle of delay α

At ωt_o the commutating voltage of valve 2 changes from the reverse to the forward direction. A regular diode cannot absorb the forward voltage, and would immediately start to conduct. However, devices such as controlled diodes have to be fired before they conduct, and they have the ability to absorb forward voltages to a certain extent according to their type. Thus, by firing the controlled diodes at angle α the current transition could be delayed. At angle α=o° the controlled diodes operate as regular diodes.

By varying α from o° to almost 180°, the output d.c. voltage is varied from a maximum positive value to a maximum negative value. In the region from maximum positive to zero output voltage, the converter is operating as a rectifier. For negative output voltage, the converter is working as an inverter.

2.2 Principles Of Pulse Timing Control

In order to control the output voltage of the phase-controlled converter, it is necessary to control the phase of the thyristor firing pulses. Many alternative principles exist for achieving this end. Some of these principles will be discussed briefly here.

2.2.1 The Cosine Wave Crossing Pulse Timing Method[1]

The basic principle, quite simply, is to determine the firing point for each thyristor from the crossing point of an associated cosine timing wave with an analog reference voltage. The cosine timing wave is derived from, and synchronized to, the converter a.c. input voltage, and

its phase is such that its peak occurs at the earliest possible commutation angle i.e. $\alpha = 0°$ of the associated thyristor.

The cosine wave crossing control principle is illustrated by the waveforms of Fig. 2.2. Each firing pulse is initiated at the point at which the associated cosine timing wave becomes instantaneously equal to the reference voltage. That is when

$$V_T \cos \theta_i = v_R \tag{2.1}$$

where

V_T = peak value of the timing wave.

v_R = value of the reference voltage.

By definition, at this instant, θ_i is equal to α, i.e.,

$$V_T \cos \alpha = v_R \tag{2.2}$$

which gives

$$\cos \alpha = \frac{v_R}{V_T} \tag{2.3}$$

2.2.1.1 Self Regulating Property

A natural feature of the cosine wave crossing timing method is that any variation in the amplitude of the timing waves, caused by a corresponding amplitude variation in the converter a.c. voltage, results in a shift of firing angle which is inherently such as to maintain a constant mean voltage at the d.c. terminals.

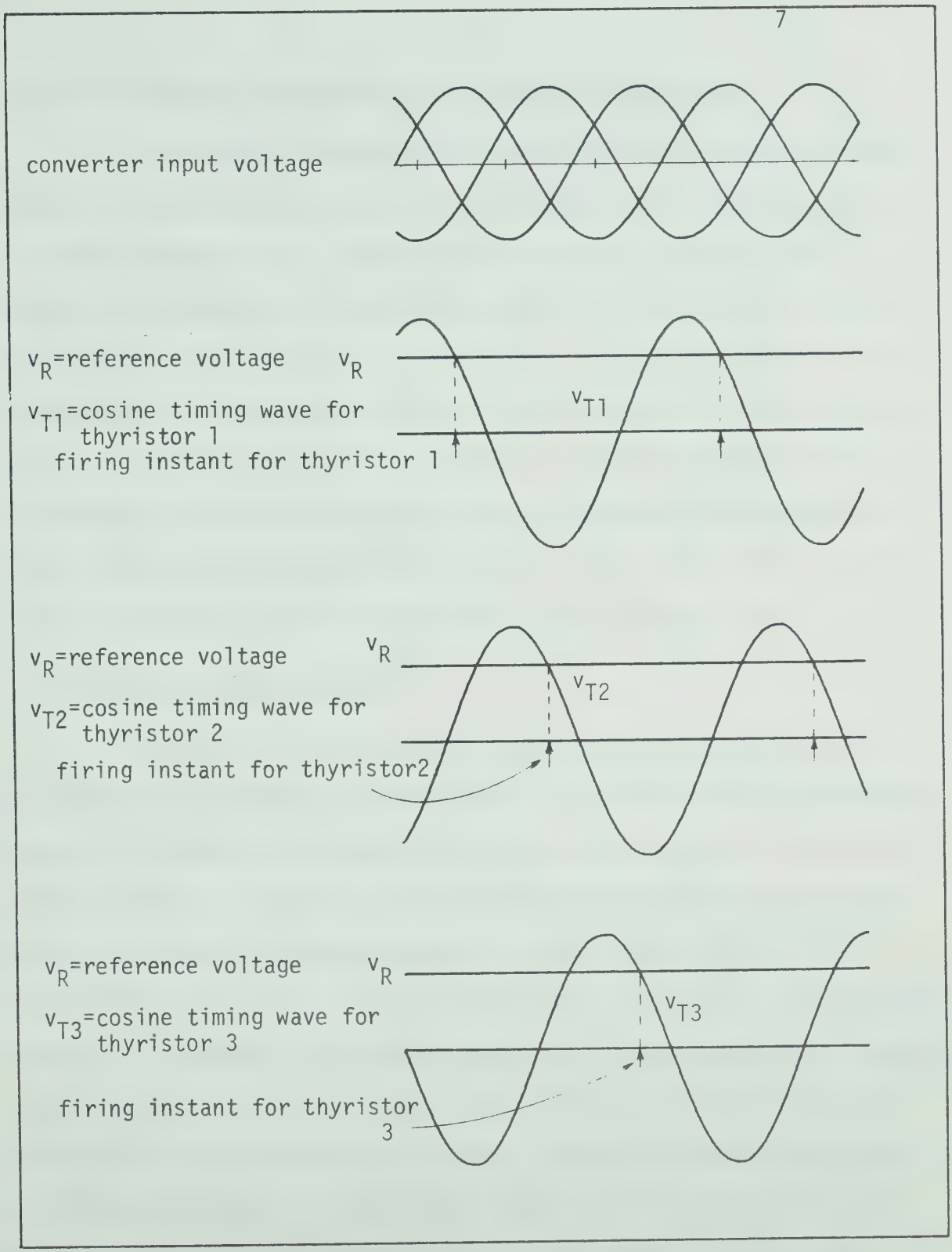


Fig. 2.2 Waveforms illustrating the basic principle of the "cosine wave crossing" control method

2.2.1.2 Presence of Distortion On The Input Voltage Waves

A practical difficulty with the cosine wave crossing control method arises from the presence of distortions, or spikes appearing on the input voltage waves. These spikes, which may originate from external disturbances on the supply system, or may be a direct result of the commutations of the converter itself, can cause spurious intersections of the timing waves with the reference voltage, thereby giving rise to incorrectly timed firing pulses. In order to overcome this difficulty, the cosine timing waves can be obtained from the converter input voltage waves through filter circuits which remove the voltage spikes and deliver smooth timing waves to the control system.

2.2.2 Integral Control Method[1]

The basic principle of the integral control method can be explained by considering a simple example in which a 6-pulse 2-quadrant converter operates at a steady firing angle, and produces a steady mean output voltage. A typical output waveform obtained with firing pulses which have perfect tracking accuracy is shown in Fig. 2.3(a). In Fig. 2.3(b) and (c) it is shown how this output voltage is comprised of a steady d.c. component with a superimposed a.c. ripply component. Examining the a.c. ripple voltage waveform, it is seen that during the interval between any two successive firing points, the net voltage-time integral of this wave is zero, in other words, the areas of waveform above and below the zero axis are exactly equal to one another. Thus, if this voltage waveform is applied to the input of an integrating circuit, the

(a) Output voltage waveform of converter

(b) Direct voltage component

(c) A.C. ripple voltage component

(d) Integrated ripple voltage waveform

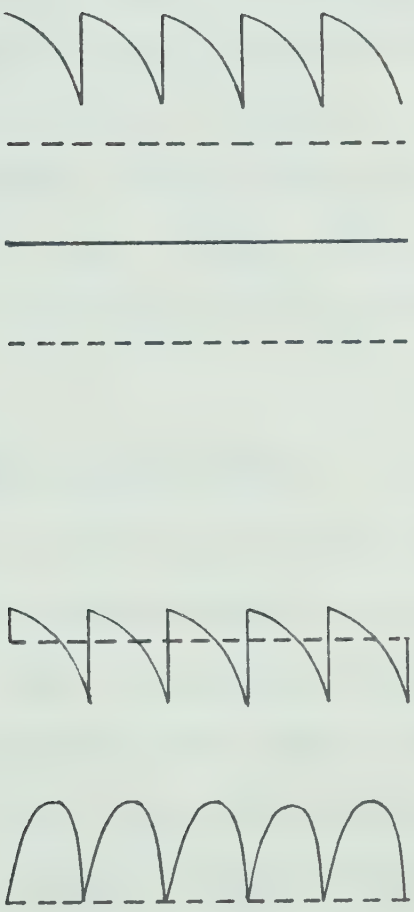


Fig. 2.3 Waveforms illustrating the basic principle of the "Integral Control" pulse timing method

output of the integrator would be instantaneously zero at each firing point, as illustrated in Fig. 2.3(d).

This phenomenon suggests that a simple timing principle is to generate a firing pulse each time the integral of the ripple voltage waveform becomes instantaneously equal to zero. The ripple voltage waveform can be obtained simply by subtracting a reference voltage from the suitably scaled actual output waveform. Thus a very tight pulse-by-pulse control is exercised over the output voltage waveform, and, in fact, this principle automatically provides a closely regulated closed-loop control of the output voltage.

2.2.2.1 Special Features Of The Integral Control Method

Since the firing pulses are generated at the zero values of the integral values of the integral of the ripple voltage, it is insensitive to changes in the supply frequency. Also, any spikes which appear on the output voltage waveform of the converter do not have any immediate or drastic effect upon the timing of the firing pulses, since the integral value of the output ripple voltage is hardly influenced by these.

A practical difficulty arises in the application of this principle for producing an alternating output voltage. In this case, the basic pulse timing control may operate apparently satisfactorily for a number of successive firing points, then the time intervals between consecutive firing pulses become more and more irregular, until finally the control is completely lost.

2.2.3 Phase-Locked Oscillator[2]

This technique for timing the firing pulses is based upon the

simple fact that under steady state conditions - with a steady d.c. output - the pulses for successive thyristors are produced at evenly spaced intervals of time. Thus, the time period between any two consecutive commutations is equal to the period of the input voltage wave, divided by the pulse number of the converter.

In theory, then, for any given steady converter firing angle, the firing instants could be timed from an independent clock pulse oscillator. This is illustrated by the waveforms of Fig. 2.4(a). The waveforms of Fig. 2.4(b) and (c) demonstrate that an increase in the clock frequency above the synchronous value results in a steadily increasing level of output voltage, by virtue of the fact that each successive firing point is relatively more advanced than the previous one, whereas a decrease in the clock frequency results in a steadily decreasing level of output voltage, because, in this case, each successive firing point is relatively more retarded than the previous one.

In practice, a negative feedback loop is used to lock the oscillator, so that its frequency and phase are forced to correspond with the desired conditions at the output of the converter. A basic feature of this pulse timing principle is its elegance and relative simplicity.

2.2.4 Commutating Voltage Integral Control Method[3]

This method is based upon the integration of the commutating

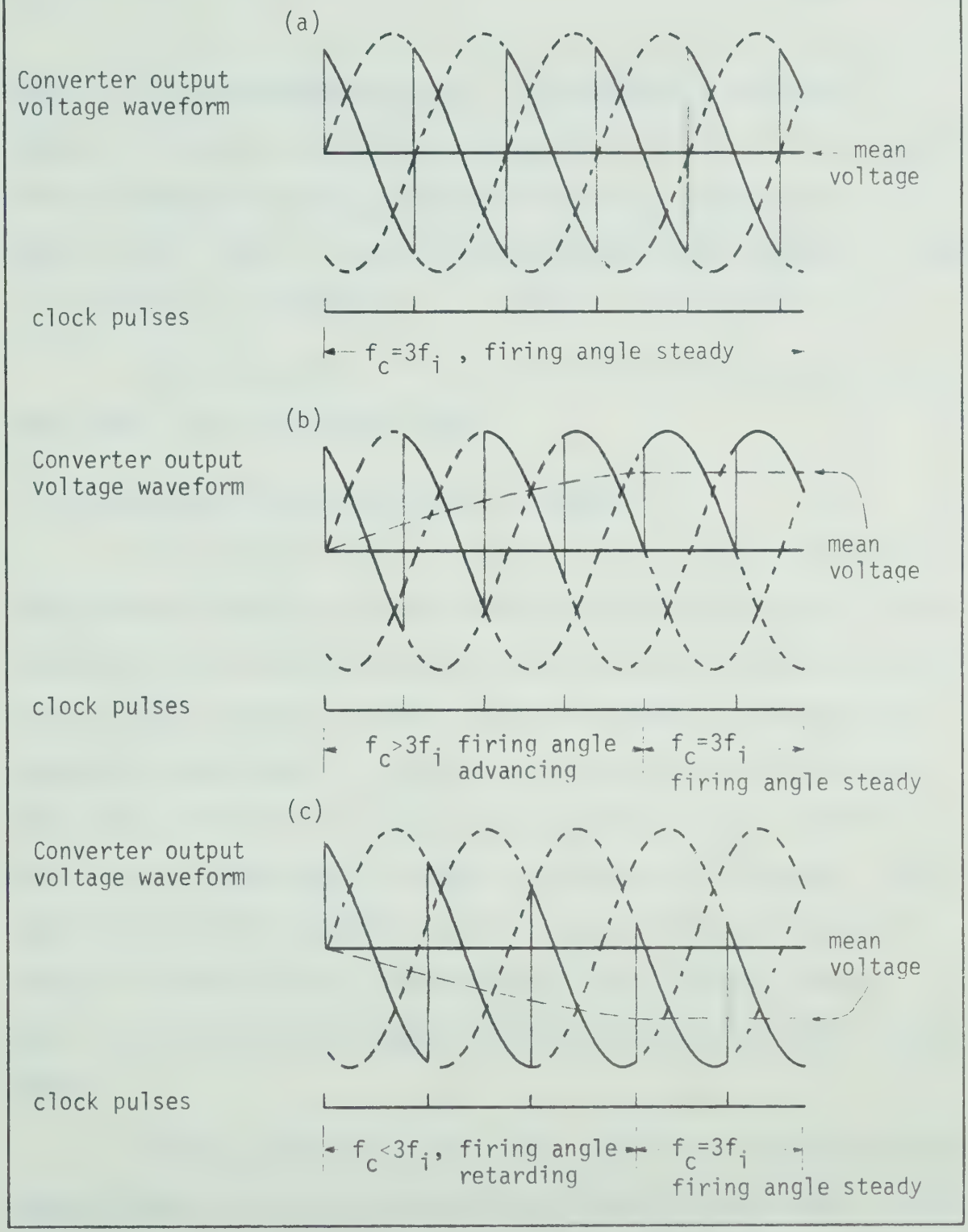


Fig. 2.4 Waveforms for a 3-pulse converter demonstrating the basic principle of the phase-locked oscillator pulse time method

voltage for the corresponding valve. This method has two special features. First, the computation is freshly carried out for each cycle and any sudden fall in a.c. voltage only affects the computation for that particular cycle. Second, the integration involved generally cancels out the effect of distortion of a.c. voltage,over the whole cycle.

Since this method is the one that will be used in this work, more details will be discussed later.

2.3 Conventional Modes Of Operation Of Converters

The technique used in applying any pulse timing principle should provide operation of the converter at the desired range. If the converter is to be operated as an inverter, a method should be provided to ensure safe inverter operation. The most commonly used control to achieve this requirement is the constant extinction angle control or CEA control. On the other hand, if the converter is to be operated as a rectifier, the scheme should include a feed-back control system. Three conventional feedback controls are mostly used; constant current (CC), constant voltage (CV), and constant power (CP), in which a feedback signal -current, voltage or power -is fed into the system as the control signal.

In some applications, it is required that the operation of the converter cover the whole range from rectification to inversion. In this case, the technique used should provide a transition from one range to the other when necessary.

A common feature in all the conventional control systems is that all valves are fired at the same angle of firing. This type of control is referred to as concurrent control.

Varying the firing angle from the maximum possible value to the minimum value, varies the output voltage from full inversion to full rectification.

CHAPTER III

A NEW METHOD OF CONTROL OF CONVERTERS

3.1 Introduction

While conventional control follows a concurrent firing angle control technique, the new control follows a consecutive one. The converter is considered as a combination of two groups. The basic principle is to control the voltage of one group from full rectification to full inversion whilst the other stays at full rectification. Over this part of the control range the combined d.c. terminal voltage is reduced from a maximum to virtually zero. In order to operate in the second quadrant, the voltage of the second group is controlled from full rectification to full inversion while the first group stays at full inversion.[5],[6]

Any of the conventional principles of pulse timing control could be used with some modification to provide the consecutive mode of operation. This could be done by providing a method for controlling each group of the converter separately. Thus, the CEA control could be applied in the inversion region in the same manner as for conventional controls. Another special feature of the new control is that the control signal is an external one, not a feedback one as in conventional controls. This will affect the operation of the converter in the

rectification region only.

3.2 Analysis Of Converter Performance Characteristics

3.2.1 Assumptions

The following simplifying assumptions are made throughout this work, unless stated otherwise.

1. Thyristors and diodes are regarded as being "ideal" circuit elements. Thus the forward voltage drop while in conduction and the leakage current while blocking are considered to be negligible. Turn-on and turn-off are considered to be instantaneous.

2. Stray circuit resistance, inductance, and capacitance are assumed to be negligible.

3. It is generally assumed, unless stated otherwise, that the current flowing at the output terminals of the converter is continuous, and perfectly smooth.

4. Whenever considering the operation of a converter power circuit it is assumed that the control equipment is capable of providing gate firing pulses with perfect tracking accuracy, the phase delay of which is controllable at will.

5. Transformers and inductors are assumed to be ideal. Thus magnetizing current, core losses, winding resistance, and leakage reactance are neglected, unless stated otherwise.

6. A.C. input voltages are assumed to be sinusoidal, and perfectly balanced, both in amplitude and in phase.

7. The details of circuit operation, the waveform diagrams, and the quantitative performance data are generally presented on the basis of the assumption of zero impedance of the a.c. source, to which the converter input terminals are connected.

3.2.2 General Features

The control scheme presented here is discussed with particular reference to the bridge connected converter, Fig. 3.1(a), although it may be used in other converter configurations. Figs. 3.1(b) and (c) show the converter operation in both the rectification and inversion regions respectively.

The 3-phase bridge converter used here which consists of 6 controlled thyristors is referred to as the 6-pulse converter.

The 3-phase converter consisting of 3 controlled thyristors will be used here as a basic unit in most of the analysis and will be referred to as 3-pulse converter.

3.2.3 Method Of Analysis[1]

The approach generally used in the harmonic analysis of phase-controlled converter circuits, is to express the complex wave in terms of a general Fourier series, the coefficient of which are then evaluated by usual methods. The basic analytical technique used in this work

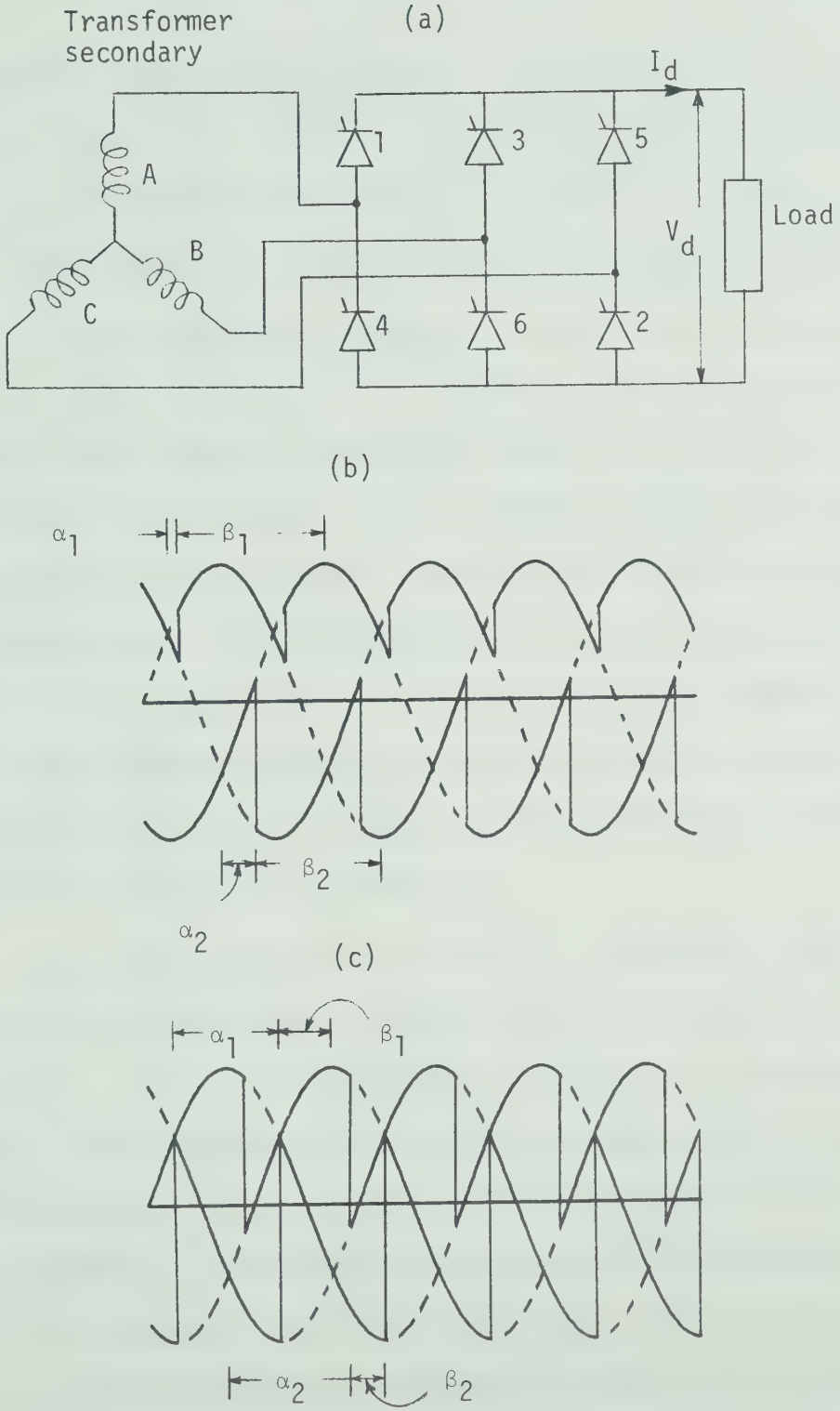


Fig. 3.1 (a) Bridge connected converter
(b) Rectifier output voltage
(c) Invertor output voltage

will not follow precisely this approach. The reason for this is that although the conventional approach can be satisfactorily applied to the analysis of converter waveforms with a steady firing angle, it is not readily applicable to the case of a consecutive mode of operation.

The basic analytical technique used here is to represent the waveforms of the voltage at the d.c. terminals, as being the sum of the individual voltage segments generated by each of the thyristors within the converter. Each individual voltage segment is expressed mathematically as the product of the appropriate sinusoidal input voltage, and a "switching function". This switching function has unity amplitude whenever the associated thyristor is on, and zero amplitude whenever it is off. By expressing each switching function as a harmonic series, the series for the d.c. terminal voltage waveform is obtained in terms of its d.c. and a.c. harmonic components.

In a similar manner the current in a given input line is represented as the sum of the individual thyristor currents associated with that line. Each thyristor current is expressed as the product of the d.c. terminal current of the associated group, and the thyristor switching function. The resulting expression obtained for the input current waveform is a complete representation of this waveform, in terms of its fundamental and harmonic components. For simplicity, the analysis is restricted to the condition of a ripple free current at the d.c. terminal. The same technique, however, could also be applied to an imperfectly smoothed d.c. terminal current.

The performance characteristics of the 3-pulse converter will be analysed. Then it will be shown how the performance characteristics of the 6-pulse converter, which is a combination of two 3-pulse groups, can be obtained directly, without returning to first principles, from the basic 3-pulse group.

3.2.4 Analysis Of The Performance Characteristics Of The 3-Pulse Group

3.2.4.1 Harmonic Analysis Of The D.C. Terminal Voltage.

The method of analysis is illustrated in Fig. 3.2. The d.c. terminal voltage is represented mathematically by:

$$v_d = V_N \sin\theta_i \times F_1(\theta_i-\alpha)+V_N \sin(\theta_i- \frac{2\pi}{3}) \times F_2(\theta_i-\alpha)+ V_N \sin(\theta_i+ \frac{2\pi}{3}) \times F_3(\theta_i-\alpha) \qquad (3.1)$$

Where $F_1(\theta_i-\alpha)$, $F_2(\theta_i-\alpha)$, $F_3(\theta_i-\alpha)$ are the switching functions associated with thyristors 1,2,3 respectively. Each of these functions has unity amplitude when its associated thyristor is on, and zero amplitude at all other times.

According to Fourier harmonic analysis, $F_1(\theta_i-\alpha)$, $F_2(\theta_i-\alpha)$, $F_3(\theta_i-\alpha)$ can be expressed in terms of the following harmonic series:

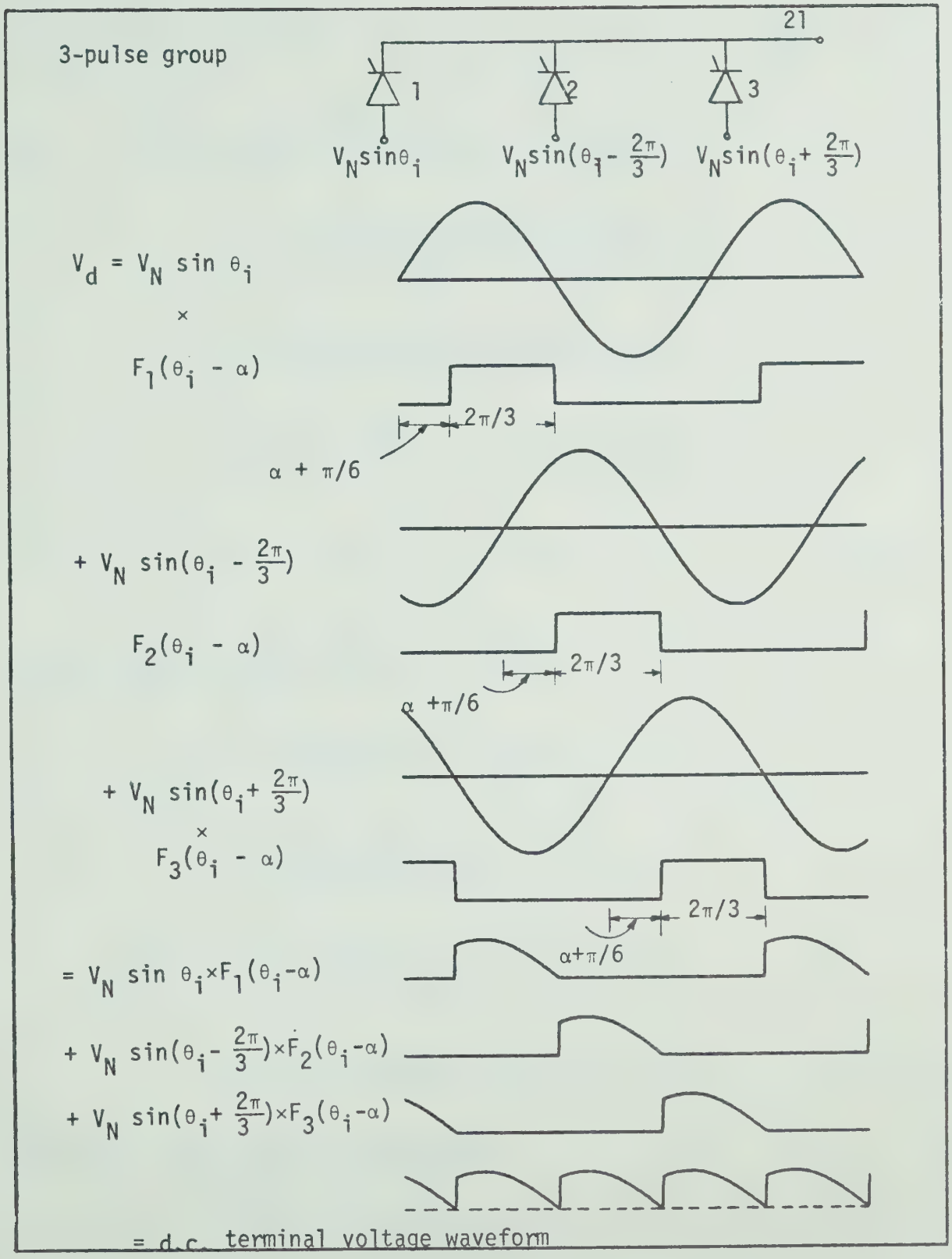


Fig. 3.2 Method of analysis of the d.c. terminal voltage waveform of the 3-pulse converter

$$F_1(\theta_i-\alpha) = \frac{1}{3} + \frac{\sqrt{3}}{\pi}\left[\sin(\theta_i-\alpha) - \frac{1}{2}\cos 2(\theta_i-\alpha)\right.$$

$$- \frac{1}{4}\cos 4(\theta_i-\alpha) - \frac{1}{5}\sin 5(\theta_i-\alpha)$$

$$- \frac{1}{7}\sin 7(\theta_i-\alpha) + \frac{1}{8}\cos 8(\theta_i-\alpha)$$

$$+ \frac{1}{10}\cos 10(\theta_i-\alpha) + \frac{1}{13}\cos 13(\theta_i-\alpha)$$

$$\left. + \ldots\right] \qquad (3.2)$$

$$F_2(\theta_i-\alpha) = \frac{1}{3} + \frac{\sqrt{3}}{\pi}\left[\sin(\theta_i-\alpha - \frac{2\pi}{3})\right.$$

$$- \frac{1}{2}\cos 2(\theta_i-\alpha - \frac{2\pi}{3})$$

$$\left. - \frac{1}{4}\cos 4(\theta_i-\alpha - \frac{2\pi}{3} - \ldots)\right] \qquad (3.3)$$

$$F_3(\theta_1-\alpha) = \frac{1}{3} + \frac{\sqrt{3}}{\pi}\left[\sin(\theta_i-\alpha + \frac{2\pi}{3})\right.$$

$$\left. - \frac{1}{2}\cos 3(\theta_i-\alpha + \frac{2\pi}{3}) \ldots\right] \qquad (3.4)$$

from (3.1), (3.2), (3.3), (3.4) we get :

$$v_d = V_N \sin\theta_1 \{ \frac{1}{3} + \frac{\sqrt{3}}{\pi} [\sin(\theta_i-\alpha) - \frac{1}{2}\cos2(\theta_i-\alpha)$$

$$- \frac{1}{4}\cos4(\theta_i-\alpha)...]\} + V_N \sin(\theta_i - \frac{2\pi}{3}) \{ \frac{1}{3}$$

$$+ \frac{\sqrt{3}}{\pi} [\sin(\theta_i-\alpha- \frac{2\pi}{3}) - \frac{1}{2}\cos2(\theta_i-\alpha- \frac{2\pi}{3})$$

$$- \frac{1}{4}\cos4(\theta_i-\alpha- \frac{2\pi}{3})...]\} + V_N \sin(\theta_i+ \frac{2\pi}{3})$$

$$\{ \frac{1}{3} + \frac{\sqrt{3}}{\pi} [\sin(\theta_i-\alpha+ \frac{2\pi}{3})...]\} \qquad (3.5)$$

By trigonometric manipulation, this reduces to

$$v_d = \frac{3\sqrt{3}}{2\pi} V_N[\cos\alpha + (\frac{1}{2^2} + \frac{1}{4^2} - \frac{2}{2.4}\cos2\alpha)^{\frac{1}{2}}$$

$$\sin(3\theta_i+\gamma_3) + (\frac{1}{5^2} + \frac{1}{7^2} - \frac{2}{5.7}\cos2\alpha)^{\frac{1}{2}}$$

$$\sin(6\theta_i+\gamma_6) + (\frac{1}{8^2} + \frac{1}{10^2} - \frac{2}{8.10}\cos2\alpha)^{\frac{1}{2}}$$

$$\sin(9\theta_i+\gamma_9) + (\frac{1}{11^2} + \frac{1}{12^2} - \frac{2}{11.12}\cos2\alpha)^{\frac{1}{2}}$$

$$\sin(12\theta_i+\gamma_{12}) + ...] \qquad (3.6)$$

$$= \frac{3\sqrt{3}}{2\pi} V_N \{\cos\alpha + \sum_{n=1}^{n=\infty} \left[\frac{1}{(3n-1)^2} + \frac{1}{(3n+1)^2} \right.$$

$$\left. - \frac{2\cos2\alpha}{(3n-1)(3n+1)} \right]^{\frac{1}{2}} \sin(3n\theta_i+\gamma_{3n}) \qquad (3.7)$$

where

$$\gamma_{3n} = -\frac{n\pi}{2} + \tan^{-1}\frac{\frac{\cos(3n+1)\alpha}{(3n+1)} - \frac{\cos(3n-1)\alpha}{3n-1}}{\frac{\sin(3n+1)\alpha}{3n+1} - \frac{\sin(3n-1)\alpha}{3n-1}} \qquad (3.8)$$

Thus, it is seen that the d.c. terminal voltage contains a steady d.c. component, $\frac{3\sqrt{3}}{2\pi}\ V_N \cos\alpha$, and an infinite (but converging) series of a.c. ripple components. The frequency of the lowest order term is three times as the input frequency, the next highest ripple frequency is six times the input frequency, and so on.

If the peak amplitude of the a.c. ripple component in the d.c. terminal voltage is plotted against the firing angle, as in Fig. 3.3, we can see that each curve is symmetrical about the 90° point. Each harmonic has its minimum value at the two extremities of the firing angle control range, and its maximum value at $\alpha = 90°$.

3.2.4.2 Harmonic Analysis Of The Input Currents

The method of analysis is illustrated in Fig. 3.4. The current in the secondary S_1 is given by:

$$i_1 = I_d \times F_1(\theta_i - \alpha)$$

$$= \frac{I_d}{3} + \frac{\sqrt{3}}{\pi}\ I_d \left[\sin(\theta_i-\alpha) - \frac{1}{2}\cos 2(\theta_i-\alpha) - \frac{1}{4}\cos 4(\theta_i-\alpha) - \frac{1}{5}\sin 5(\theta_i-\alpha) - \frac{1}{7}\sin 7(\theta_i-\alpha)\ldots\right] \qquad (3.9)$$

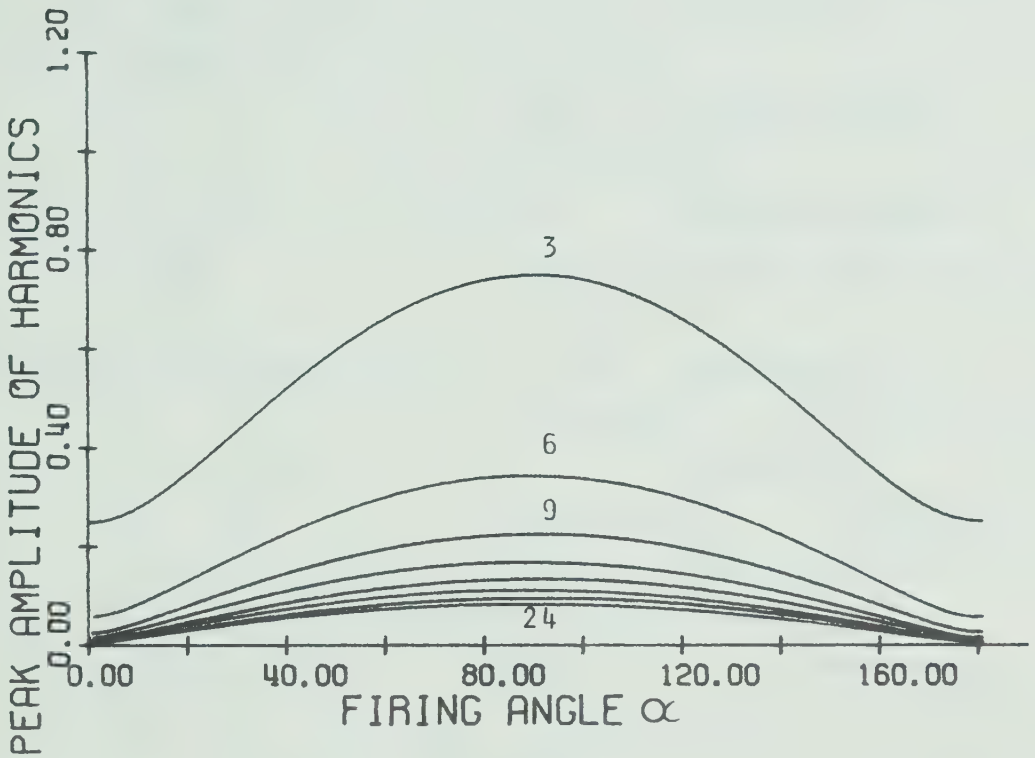


Fig. 3.3 Variation with firing angle of the harmonic components present in the d.c. terminal voltage of 3-pulse converter

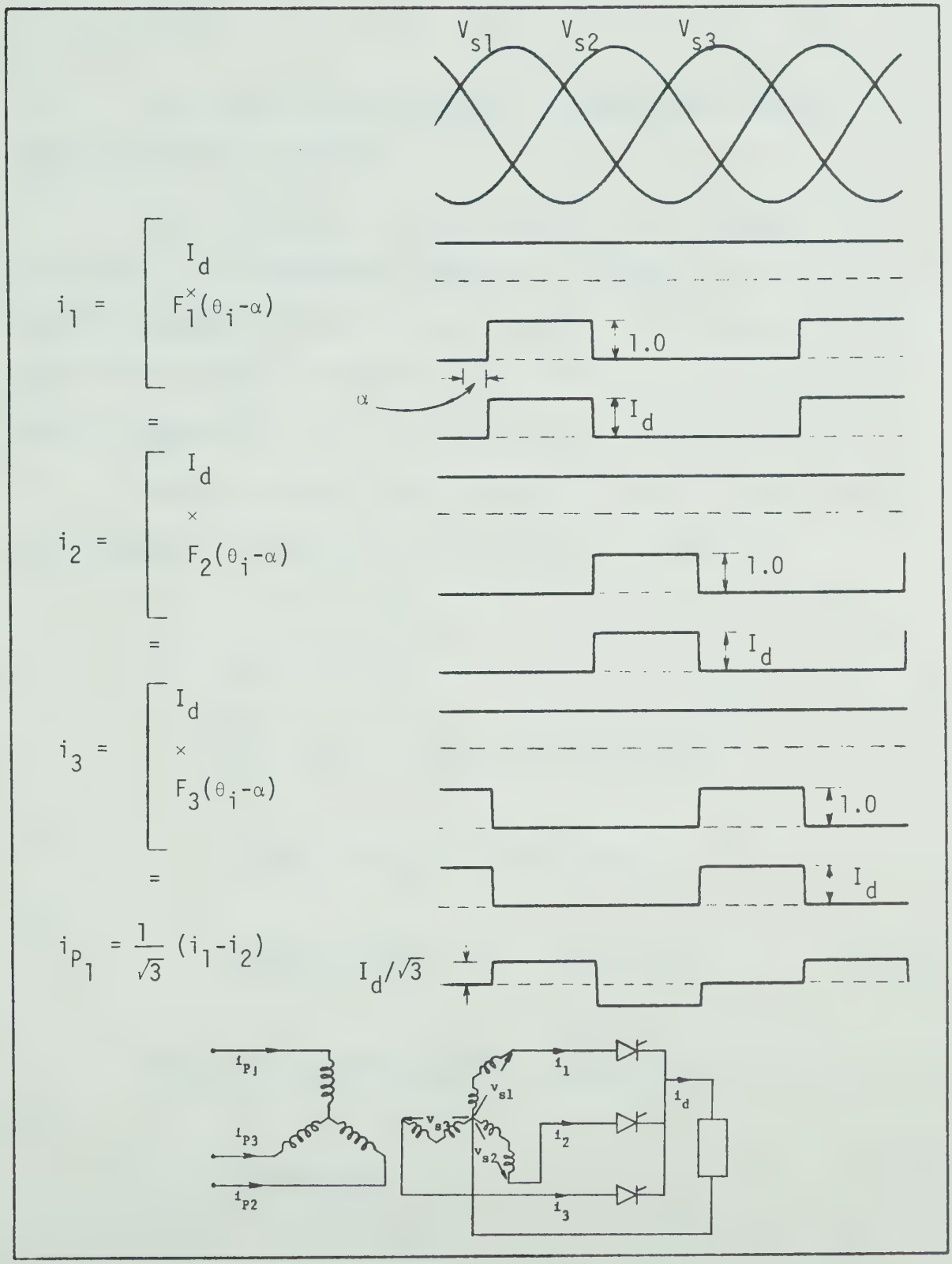


Fig. 3.4 Method of Analysis of input currents of the 3-pulse converter

The currents i_2, i_3 in S_2 and S_3 respectively could be obtained in a similar manner.

Thus the secondary current contains a d.c. component of amplitude $I_d/3$, a fundamental component of amplitude $\sqrt{3}\ I_d/\pi$ which lags the secondary voltage by an angle equal to the converter firing angle α. In addition, it contains a converging series of superimposed harmonic components.

Assuming the same line-to-neutral voltage at either side of the transformer, the current in the primary P_1 is given by:

$$
\begin{aligned}
i_{P_1} &= \frac{1}{\sqrt{3}} (i_1 - i_2) \\
&= \frac{\sqrt{3} I_d}{\pi} \left[\sin(\theta_i - \alpha + \tfrac{\pi}{6}) - \tfrac{1}{2} \cos(2\theta_i - 2\alpha - \tfrac{\pi}{6}) \right. \\
&\quad - \tfrac{1}{4} \cos(4\theta_i - 4\alpha + \tfrac{\pi}{6}) - \tfrac{1}{5} \sin(5\theta_i - 5\alpha - \tfrac{\pi}{6}) \\
&\quad \left. - \tfrac{1}{7} \sin(7\theta_i - 7\alpha + \tfrac{\pi}{6}) \ldots \right] \qquad (3.10)
\end{aligned}
$$

The associated primary line to neutral voltage is given by:

$$v_{P_1} = V_N \sin(\theta_1 + \tfrac{\pi}{6}) \qquad (3.11)$$

Thus the primary line current contains a fundamental component of amplitude $\sqrt{3}\ I_d/\pi$, which lags the primary line to neutral voltage by an angle equal to the firing angle α. In addition, it contains a converging series of superimposed harmonic components, the frequencies and relative amplitudes of which are the same as those of the secondary current waveform.

3.2.5 Analysis Of The Performance Characteristics Of The 6-Pulse Converter

3.2.5.1 Harmonic Analysis Of The D.C. Terminal Voltage

Considering the 6-pulse converter as a combination of two 3-pulse groups, the d.c. terminal voltage is synthesized from the individual voltages $v_{d_{31}}$ and $v_{d_{32}}$ of the two 3-pulse groups

$$v_d = v_{d_{31}} + v_{d_{32}} \tag{3.12}$$

where:

$$v_{d_{31}} = \frac{3\sqrt{3}}{2\pi}\ V_N \left[\cos\alpha_1 + \left(\frac{1}{2^2} + \frac{1}{4^2} - \frac{2\cos 2\alpha_1}{2.4} \right)^{\frac{1}{2}} \right.$$

$$\sin 3(\theta_i + \gamma_3) + \left(\frac{1}{5^2} + \frac{1}{7^2} - \frac{2\cos 2\alpha_1}{5.7} \right)^{\frac{1}{2}}$$

$$\left. \sin 6(\theta_i + \gamma_3) + \ldots \right] \tag{3.13}$$

and since the input a.c. voltage of the second group is in effect displaced by 180° from that for the first group, then the d.c. terminal

voltage of group 2 is obtained by replacing $(\theta_i+\pi)$ for θ_i and α_2 for α_1 in equation (3.13) to get:

$$v_{d_{32}} = \frac{3\sqrt{3}}{2\pi} V_N \left[\cos\alpha_2 - \left(\frac{1}{2^2} + \frac{1}{4^2} - \frac{2\cos 2\alpha_2}{2.4} \right)^{\frac{1}{2}} \right.$$

$$\sin(3\theta_i+\bar{\gamma}_3) + \left(\frac{1}{5^2} + \frac{1}{7^2} - \frac{2\cos 2\alpha_2}{5.7} \right)^{\frac{1}{2}}$$

$$\left. \sin(6\theta_i+\bar{\gamma}_6) + \ldots \right] \qquad (3.14)$$

Hence the final d.c. terminal voltage of the 6-pulse group is given by

$$v_d = \frac{3\sqrt{3}}{2\pi} V_N \left[\cos\alpha_1 + \cos\alpha_2 + \left(\frac{1}{2^2} + \frac{1}{4^2} - \frac{2\cos 2\alpha_1}{2.4} \right)^{\frac{1}{2}} \right.$$

$$\sin(3\theta_i+\gamma_3) - \left(\frac{1}{2^2} + \frac{1}{4^2} - \frac{2\cos 2\alpha_2}{2.4} \right)^{\frac{1}{2}}$$

$$\sin(3\theta_i+\bar{\gamma}_3) + \left(\frac{1}{5^2} + \frac{1}{7^2} - \frac{2\cos 2\alpha_1}{5.7} \right)^{\frac{1}{2}}$$

$$\sin(6\theta_i+\gamma_6) + \left(\frac{1}{5^2} + \frac{1}{7^2} - \frac{2\cos 2\alpha_2}{5.7} \right)^{\frac{1}{2}}$$

$$\left. \sin(6\theta_i+\bar{\gamma}_6) + \ldots \right] \qquad (3.15)$$

$$= \frac{3\sqrt{3}}{2\pi} V_N \{\cos\alpha_1+\cos\alpha_2+ \sum_{n=1}^{\infty} \left[\left(\frac{1}{(3n-1)^2} + \frac{1}{(3n+1)^2} \right.\right.$$

$$\left. - \frac{2\cos 2\alpha_1}{(3n+1)(3n-1)} \right)^{\frac{1}{2}} \sin(3n\theta_i+\gamma_{3n}) \Big] + (-1)^n \left[\left(\frac{1}{(3n-1)^2} \right.\right.$$

$$\left. + \frac{1}{(3n+1)^2} - \frac{2\cos 2\alpha_2}{(3n+1)(3n-1)} \right)^{\frac{1}{2}} \sin(3n\theta_i+\bar{\gamma}_{3n}) \Big] \} \quad (3.16)$$

By trigonometric manipulation, this can be written as:

$$v_d = \frac{3\sqrt{3}V_N}{2\pi} \{ \cos\alpha_1+\cos\alpha_2+ \sum_{n=1}^{\infty} \left[(A_n\cos\gamma_{3n}+B_n\cos\bar{\gamma}_{3n})^2 \right.$$

$$\left. + (A_n\sin\gamma_{3n}+B_n\sin\bar{\gamma}_{3n})^2 \right]^{\frac{1}{2}} \sin(3n\theta_i+\zeta_{3n}) \} \quad (3.17)$$

where

$$A_n = \left(\frac{1}{(3n-1)^2} + \frac{1}{(3n+1)^2} - \frac{2\cos 2\alpha_1}{(3n-1)(3n+1)} \right)^{\frac{1}{2}} \quad (3.18),$$

$$B_n = \left(\frac{1}{(3n-1)^2} + \frac{1}{(3n+1)^2} - \frac{2\cos 2\alpha_2}{(3n-1)(3n+1)} \right)^{\frac{1}{2}} \times(-1)^n \quad (3.19),$$

$$\gamma_{3n} = -\frac{n\pi}{2} + \tan^{-1} \frac{\frac{\cos(3n+1)\alpha_1}{3n+1} - \frac{\cos(3n-1)\alpha_1}{3n-1}}{\frac{\sin(3n+1)\alpha_1}{3n+1} - \frac{\sin(3n-1)\alpha_1}{3n-1}} \quad (3.20),$$

$$\bar{\gamma}_{3n} = -\frac{n\pi}{2} + \tan^{-1} \frac{\frac{\cos(3n+1)\alpha_2}{3n+1} - \frac{\cos(3n-1)\alpha_2}{3n-1}}{\frac{\sin(3n+1)\alpha_2}{3n+1} - \frac{\sin(3n-1)\alpha_2}{3n-1}} \quad (3.21)$$

$$\zeta_{3n} = \tan^{-1} \frac{A_n \sin \gamma_{3n} + B_n \sin \bar{\gamma}_{3n}}{A_n \cos \gamma_{3n} + B_n \cos \bar{\gamma}_{3n}} \qquad (3.22)$$

Thus it is seen that the d.c. terminal voltage contains a steady d.c. component $= \frac{3\sqrt{3}V_N}{2\pi} (\cos\alpha_1 + \cos\alpha_2)$, and an infinite (but converging) series of a.c. ripple components.

To get the d.c. terminal voltage for conventional control we put $\alpha_1 = \alpha_2 = \alpha$ in equations (3.16), (3.17), (3.18), (3.19) and (3.20) we get:

$$A_n = (-1)^n \quad B_n = \frac{1}{(3n-1)^2} + \frac{1}{(3n+1)^2} - \frac{2\cos 2\alpha}{(3n-1)(3n+1)} \qquad (3.23),$$

$$\gamma_{3n} = \bar{\gamma}_{3n} = \zeta_{3n} = -\frac{n\pi}{2} + \tan^{-1} \frac{\frac{\cos(3n+1)\alpha}{3n+1} - \frac{\cos(3n-1)\alpha}{3n-1}}{\frac{\sin(3n+1)\alpha}{3n+1} - \frac{\sin(3n-1)\alpha}{3n-1}} \qquad (3.24),$$

And
$$v_d = \frac{3\sqrt{3}\, V_N}{\pi} \{\cos\alpha + \sum_{n=1}^{\infty} \left(\frac{1}{(6n-1)^2} + \frac{1}{(6n+1)^2} - \frac{2\cos 2\alpha}{(6n-1)(6n+1)} \right)^{\frac{1}{2}}$$

$$\sin(6n\theta_i + \gamma_{6n})\} \qquad (3.25)$$

The d.c. component here is equal to:

$$\frac{3\sqrt{3}V_N}{\pi} (\cos\alpha)$$

3.2.6 Output Voltage Waveforms[4]

A simplified technique is used here for obtaining the output voltage waveforms of the 6-pulse converter. This technique is similar to that used in the previous analysis. The converter is considered consisting of two groups; positive group - the upper valves - and negative one - the lower valves. The line to neutral output d.c. voltage is obtained for each group separately and then the summation of these two waveforms will give the total output voltage waveforms. Figs. 3.5 - 11 shows the total output waveforms for different values of firing angles α_1 and α_2. These plots were obtained using the Calcomp plotter at the University of Alberta Computing Center.

Output voltage waveforms for conventional controls are also obtained using the same technique for $\alpha_1 = \alpha_2$. Figs. 3.13 - 17.

3.2.7 A.C. Ripple Components In The D.C. Terminal Voltage

From (3.17), (3.18), (3.19), (3.20), (3.21) and (3.22), the relation between the peak amplitudes of the a.c. ripple components in the d.c. terminal voltage, and the firing angles α_1 and α_2 could be obtained. Figs. 3.18,19 show these relations up to the 24th harmonic of the input frequency.

Comparison between these curves and those obtained for conventional control Fig. 3.20 yields the following comments.

1. It is clear that the harmonic contents in the output d.c.

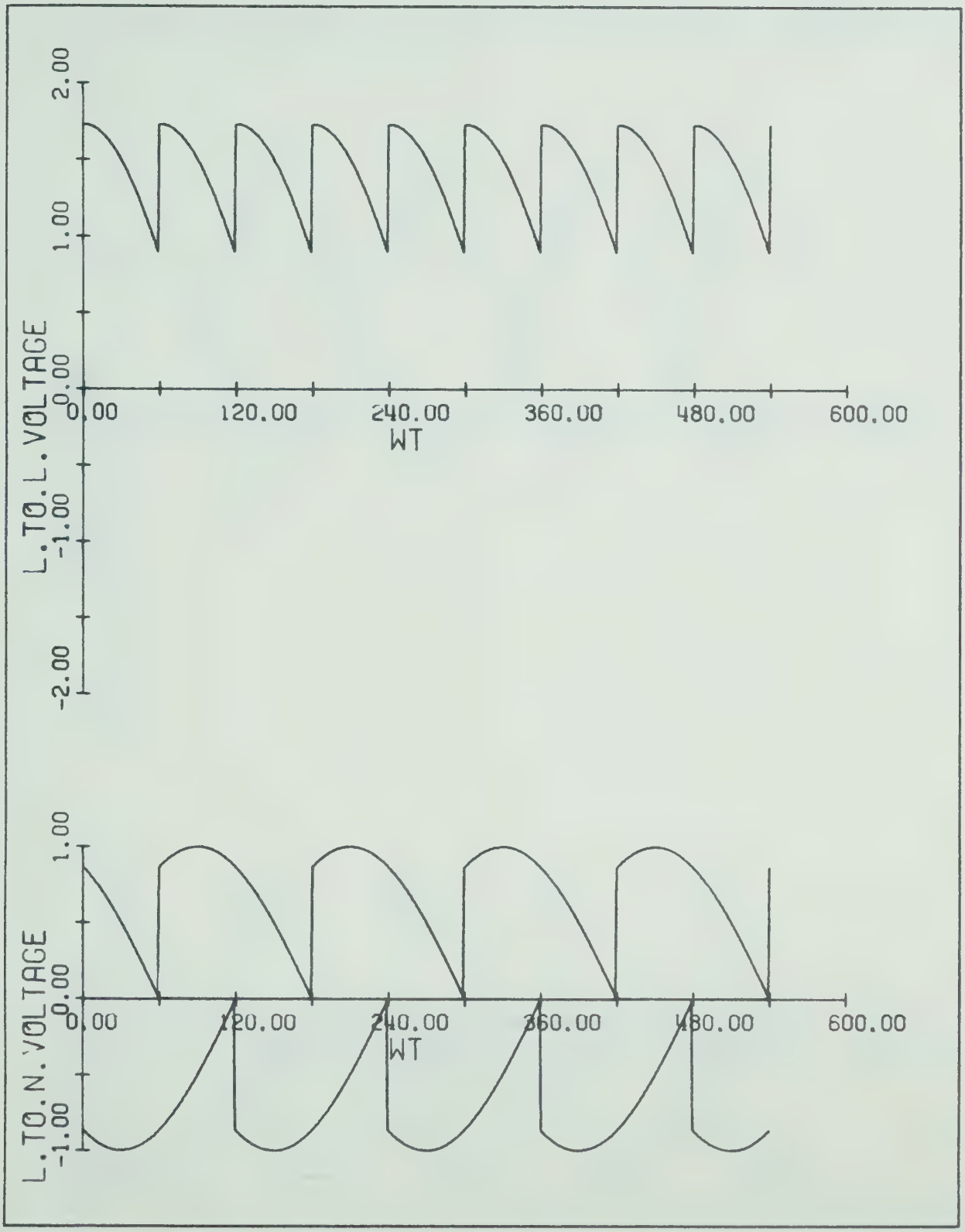


Fig. 3.5 D.C. output voltage waveform using the new control for α_1=30°, α_2=30°

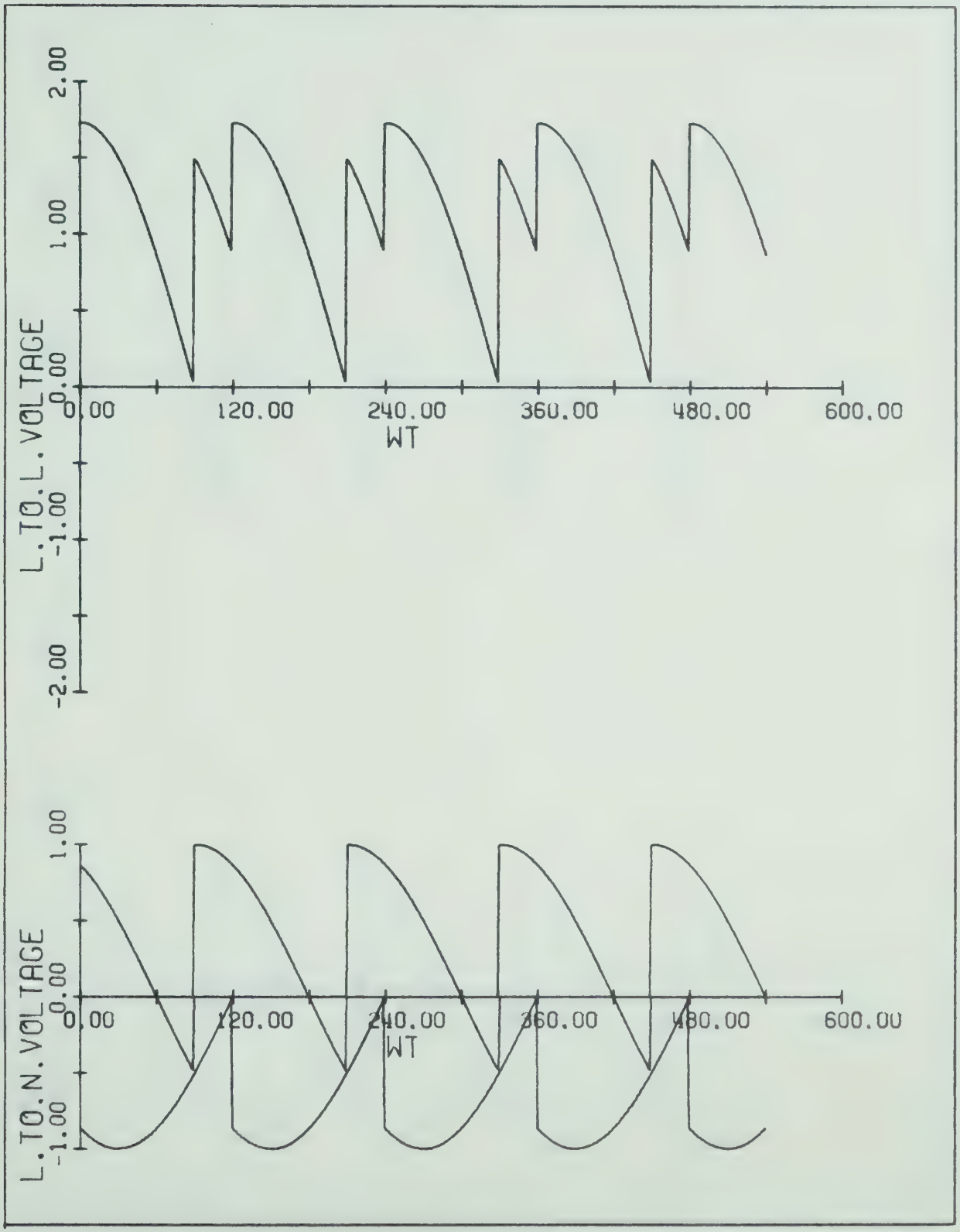


Fig. 3.6 D.C. output voltage waveform using the new control for α_1=60°, α_2=30°

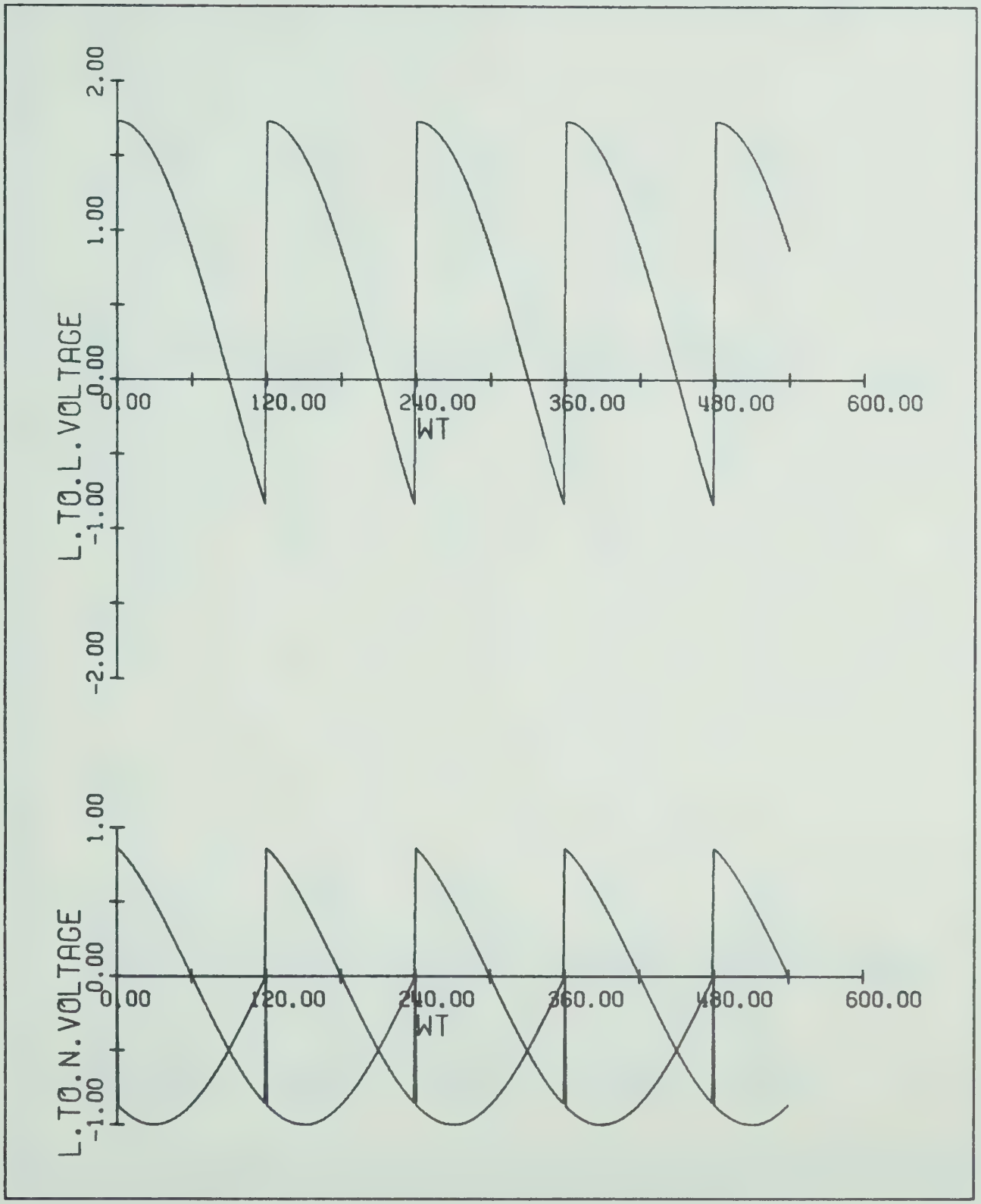


Fig. 3.7 D.C. output voltage waveform using the new control for $\alpha_1=90°$, $\alpha_2=30°$

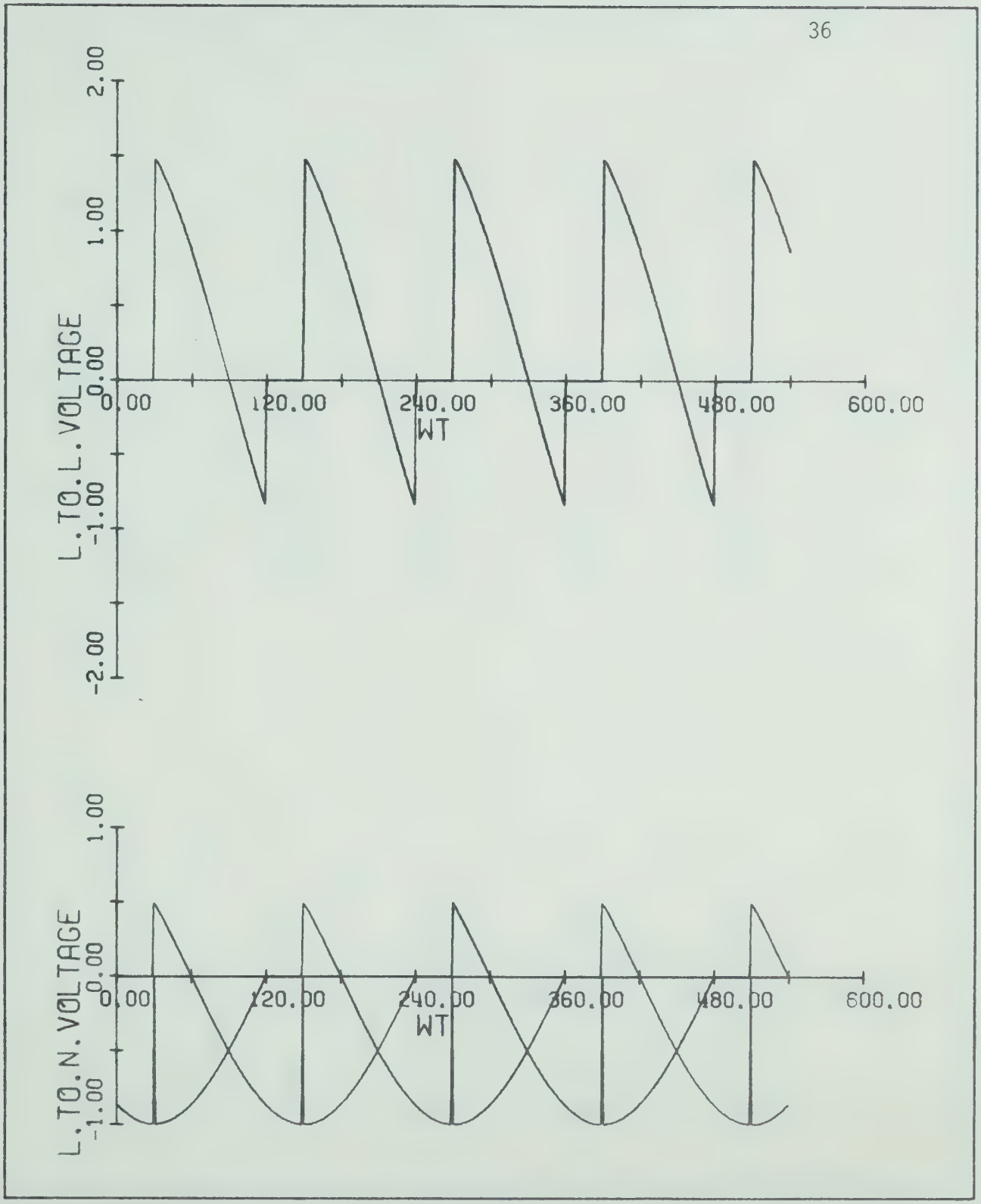


Fig. 3.8 D.C. output voltage waveform using the new control for α_1=120°, α_2=30°

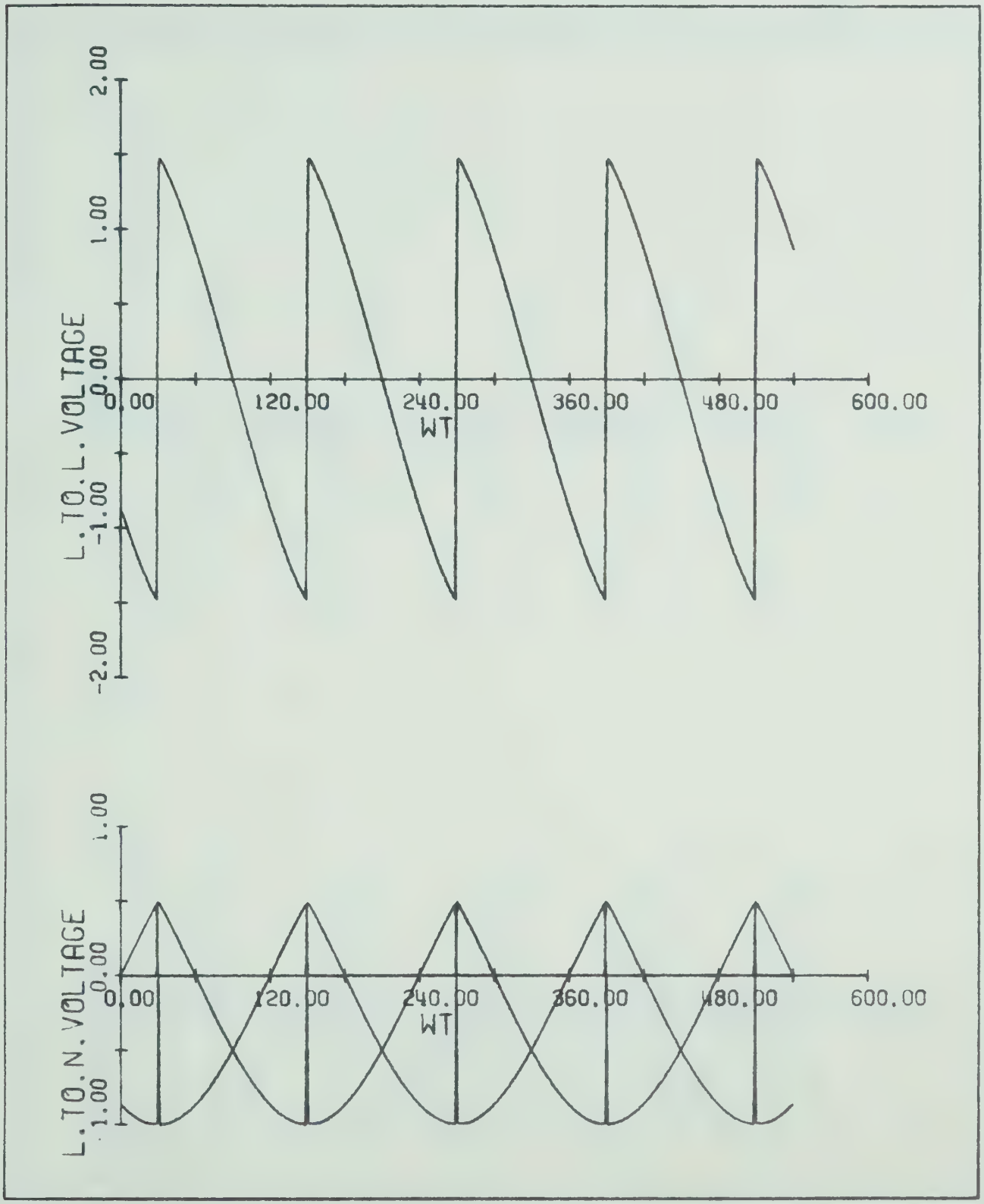


Fig. 3.9 D.C. output voltage waveform using the new control for α_1=120°, α_2=60°
(Zero output voltage)

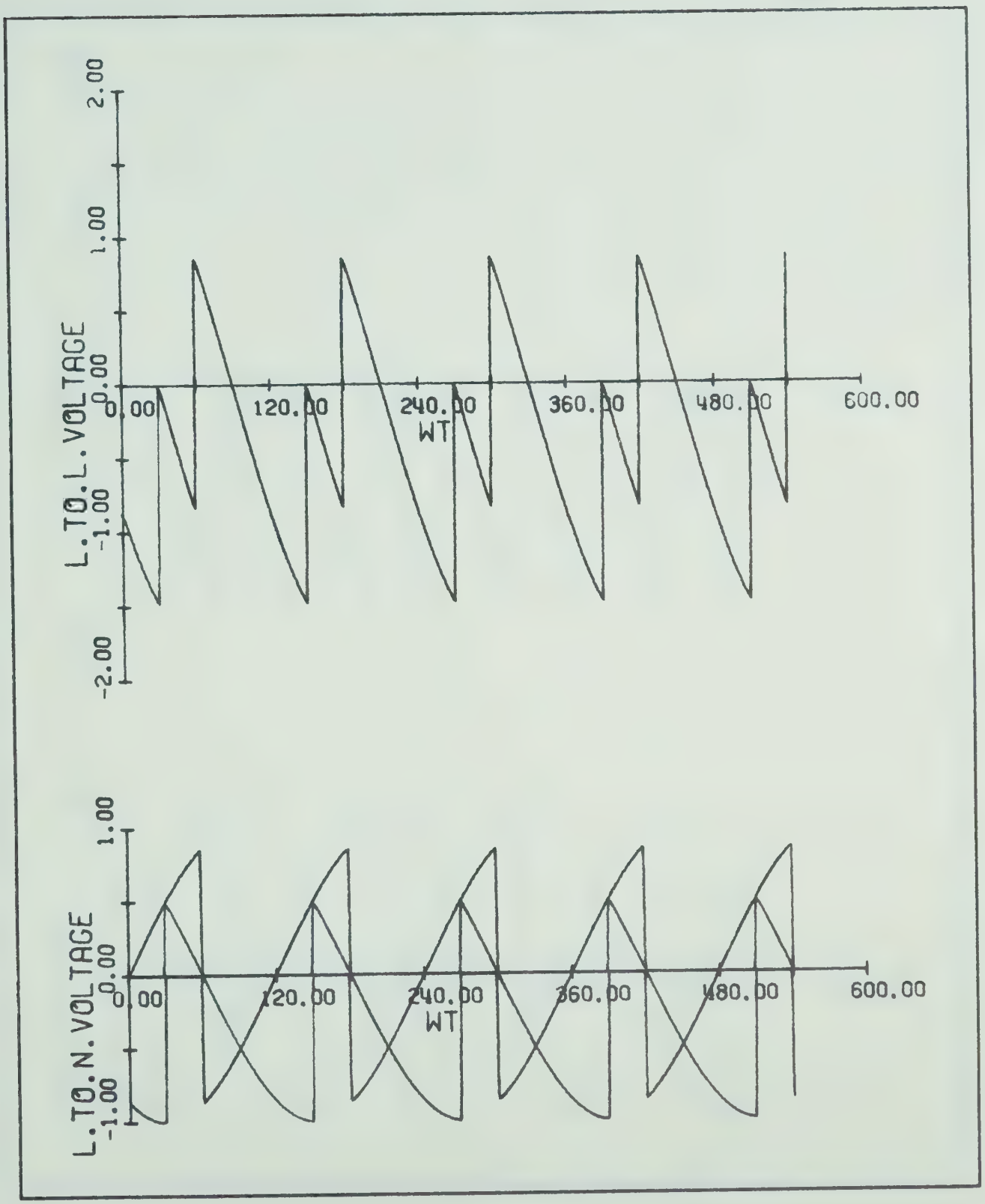


Fig. 3.10 D.C. output voltage waveform using the new control for α_1=120°, α_2=90°

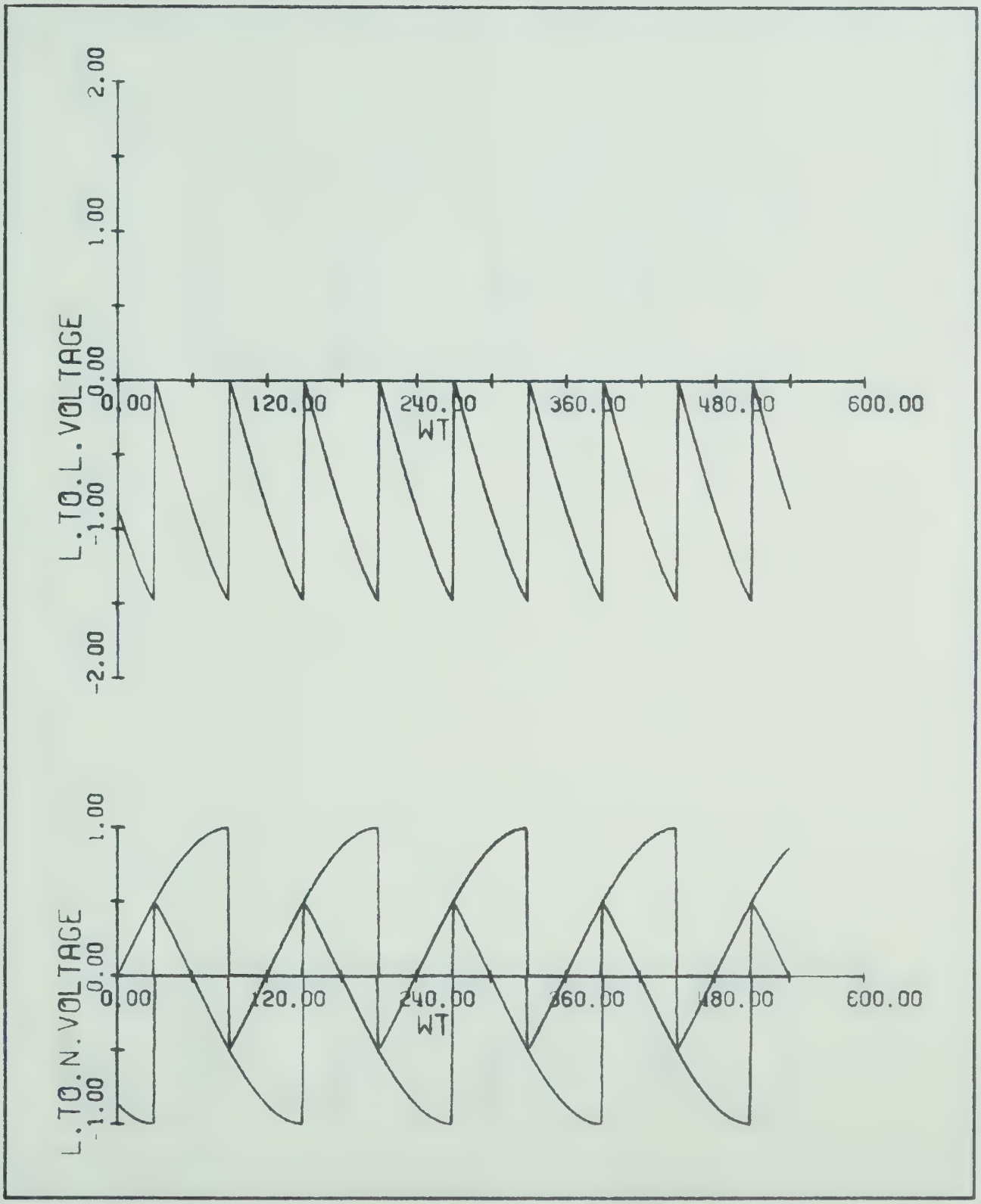


Fig. 3.11 D.C. output voltage waveform using the new control for α_1=120°, α_2=120°

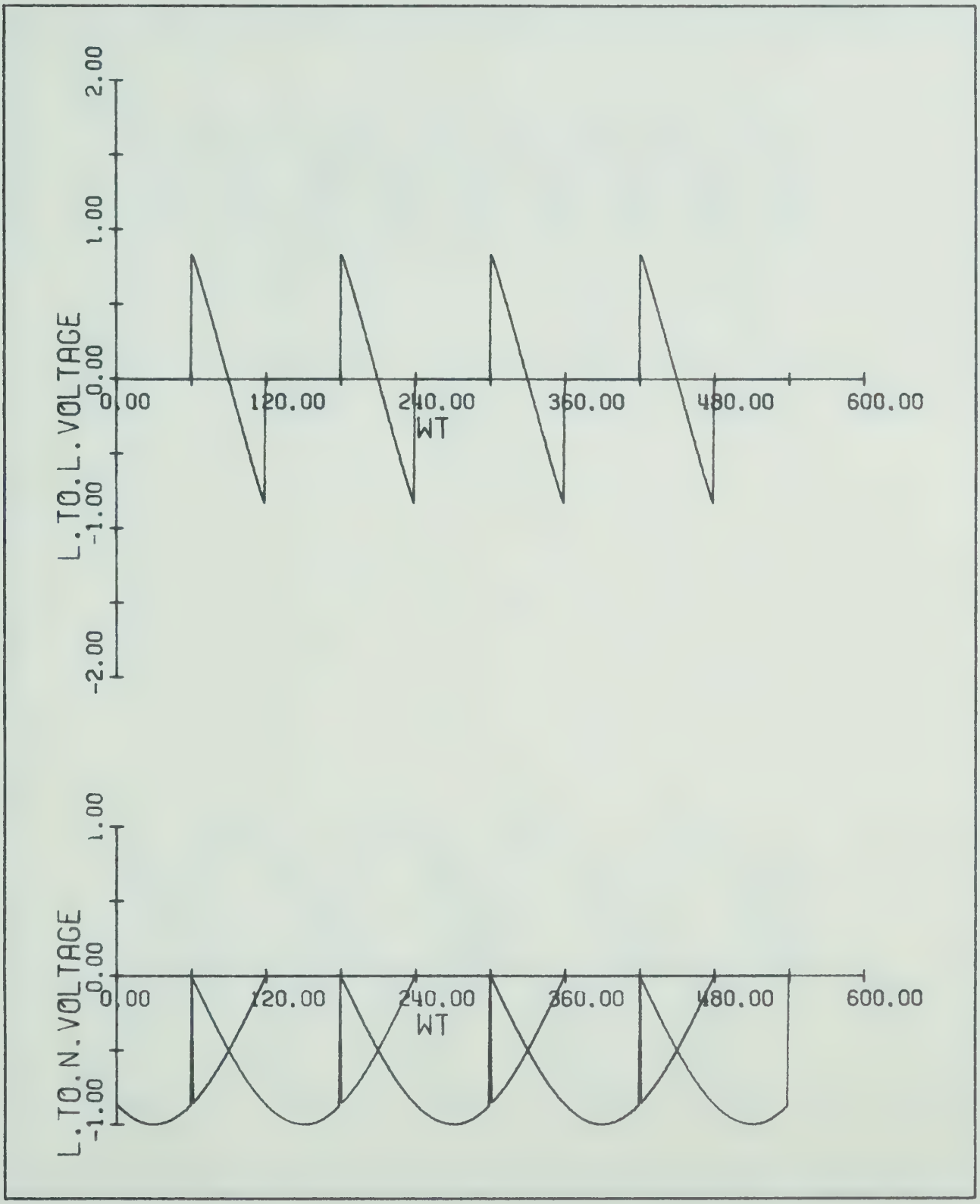


Fig. 3.12 D.C. output voltage waveform using the new control for α_1=150°, α_2=30°

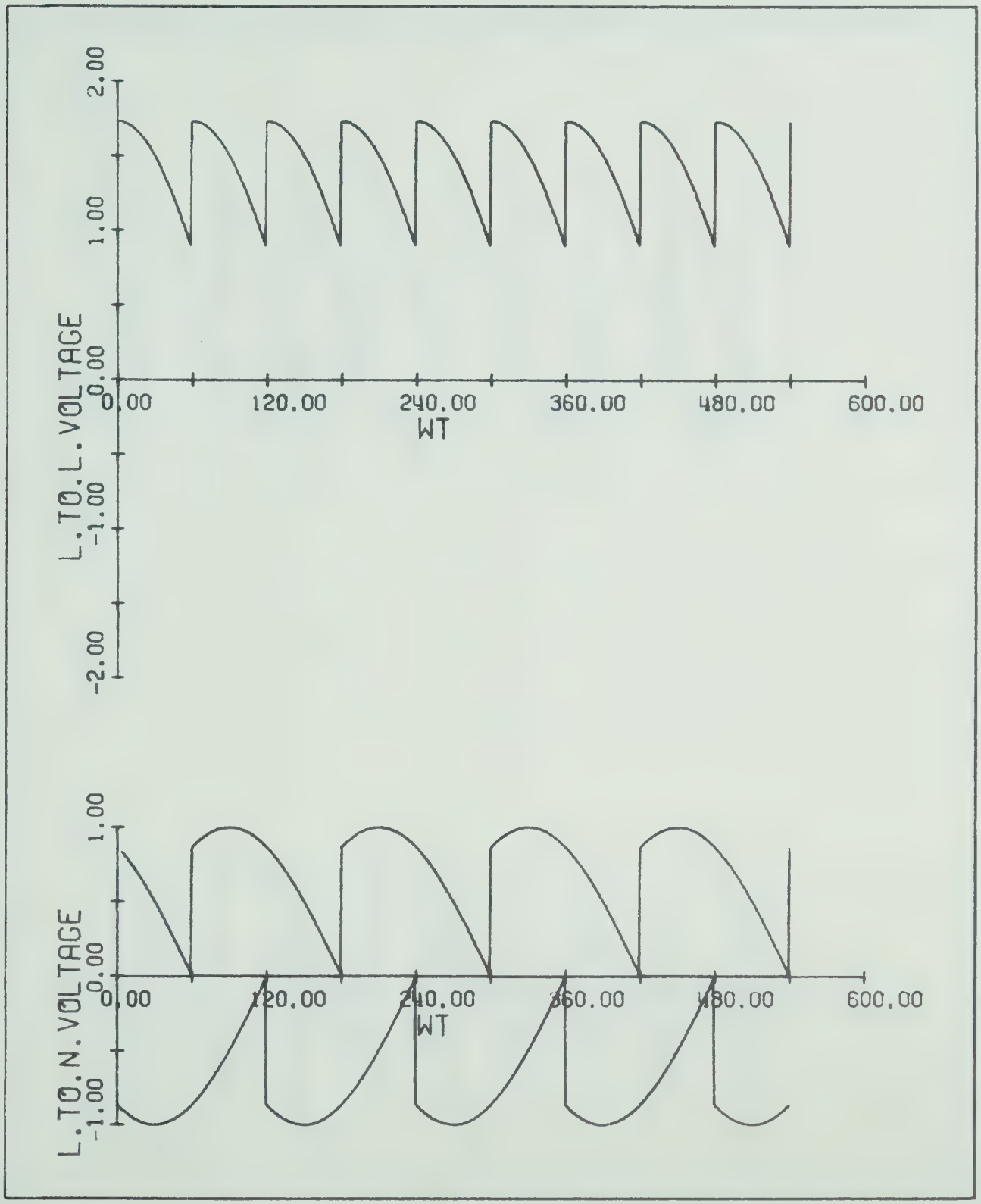


Fig. 3.13 D.C. output voltage waveform using conventional control for $\alpha = 30°$

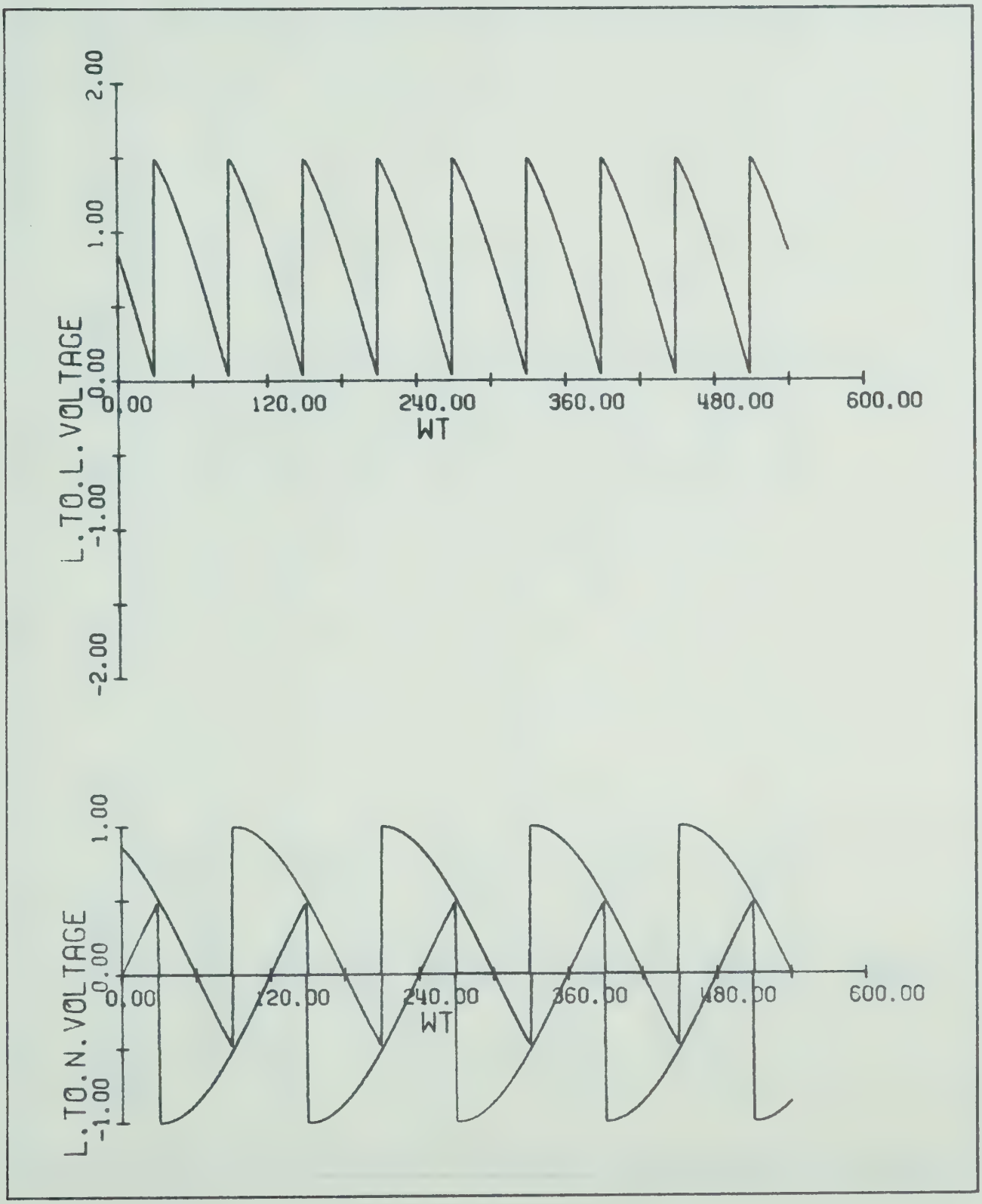


Fig. 3.14 D.C. output voltage waveform using conventional control for $\alpha = 60°$

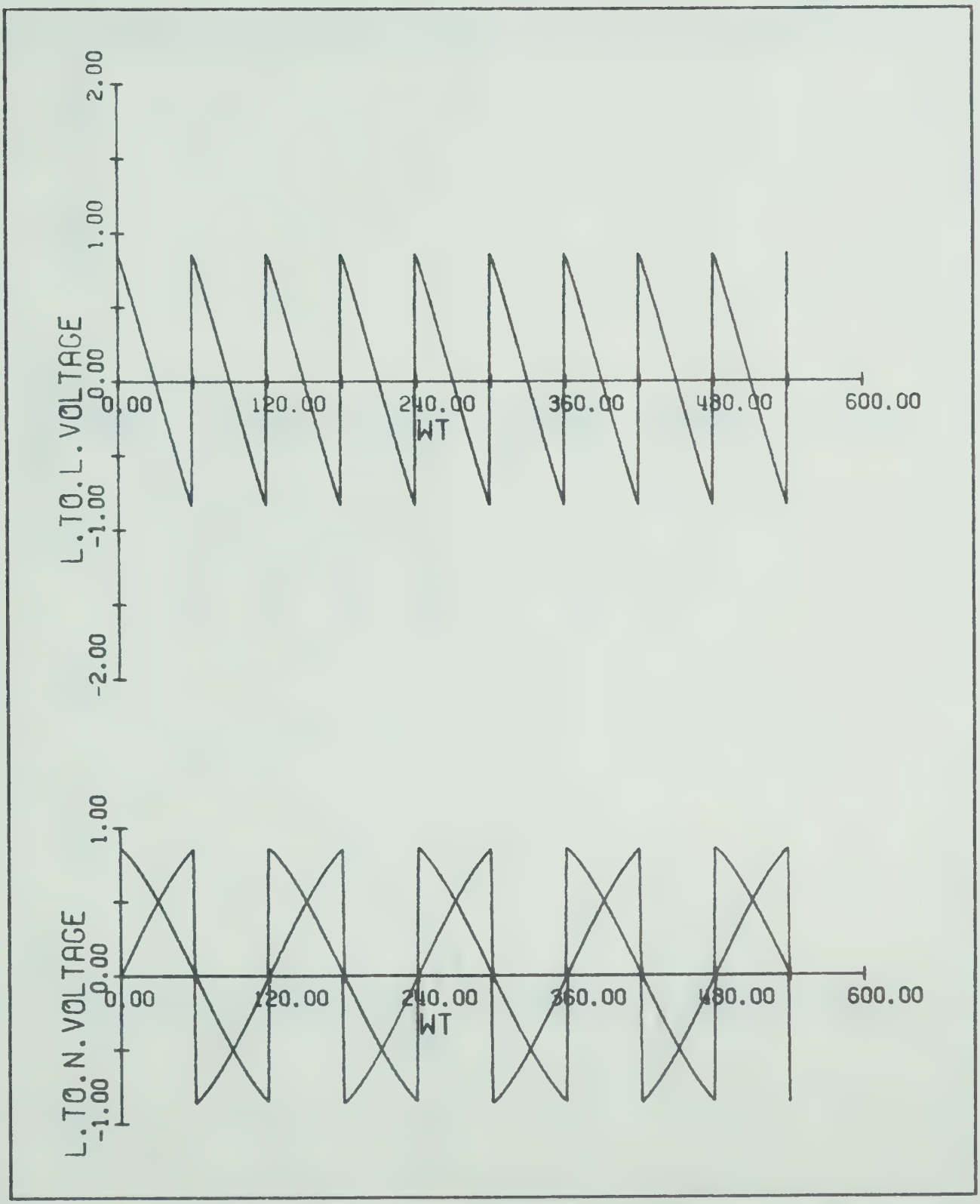


FIg. 3.15 D.C. output voltage waveform using conventional control for $\alpha = 90°$ (Zero output voltage)

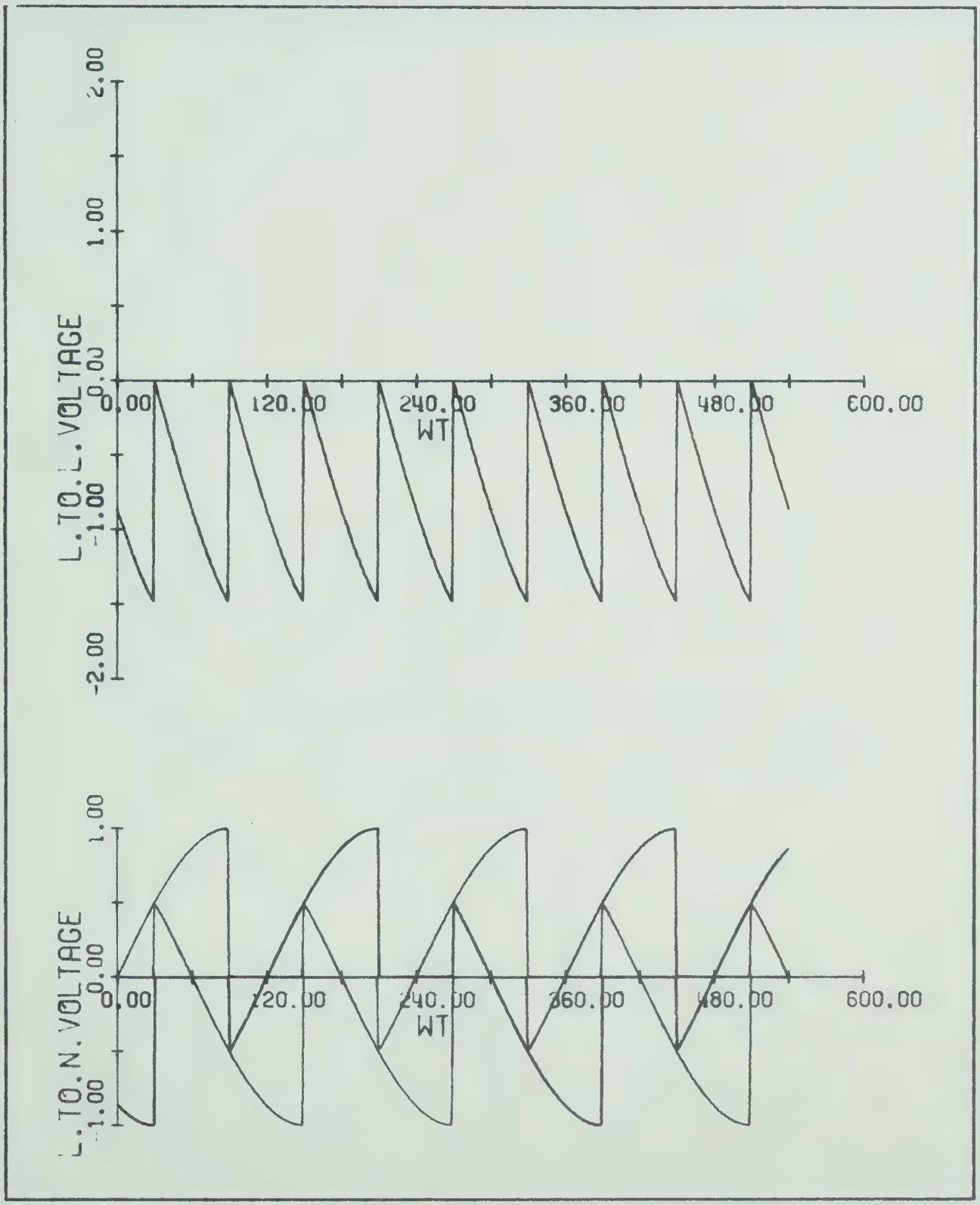


Fig. 3.16 D.C. output voltage waveform using conventional control for $\alpha = 120°$

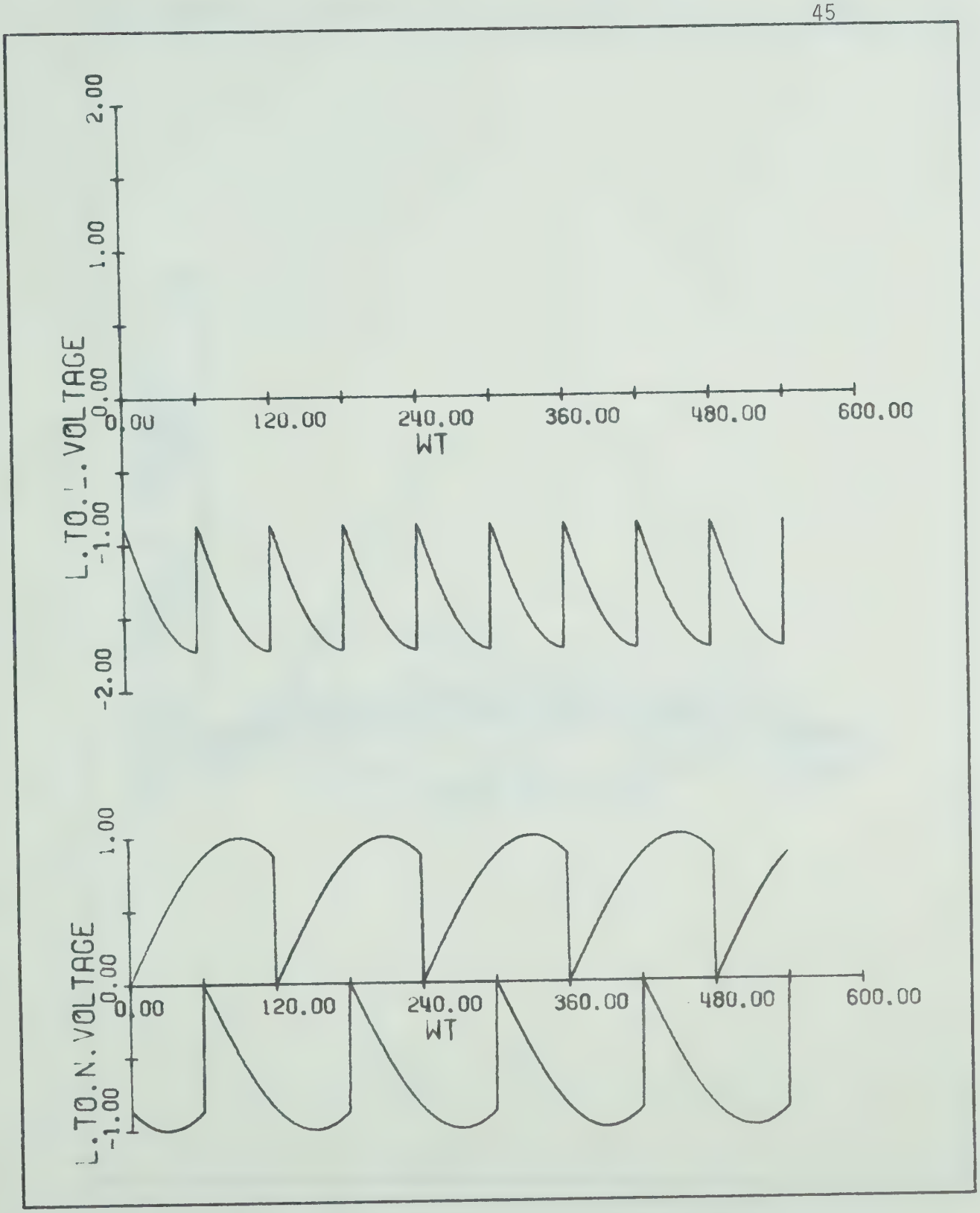


Fig. 3.17 D.C. output voltage waveform using conventional control for $\alpha = 150°$

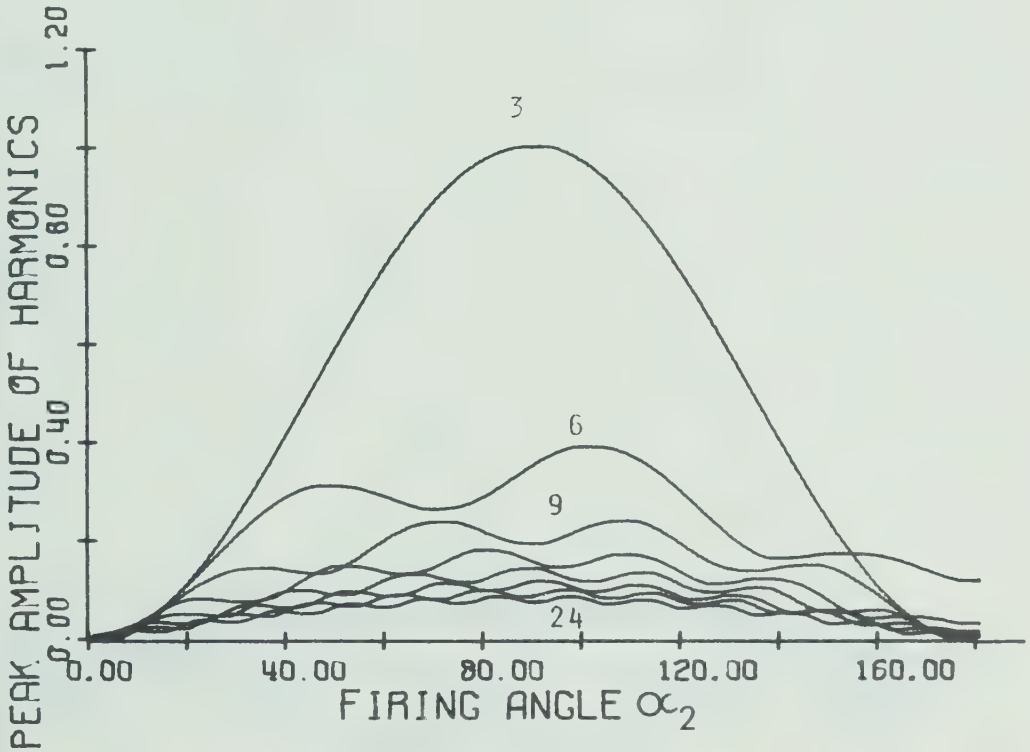


Fig. 3.18 Harmonic contents in d.c. terminal voltage for a 6-pulse converter using the new control for α_1=175° α_2=0-180°

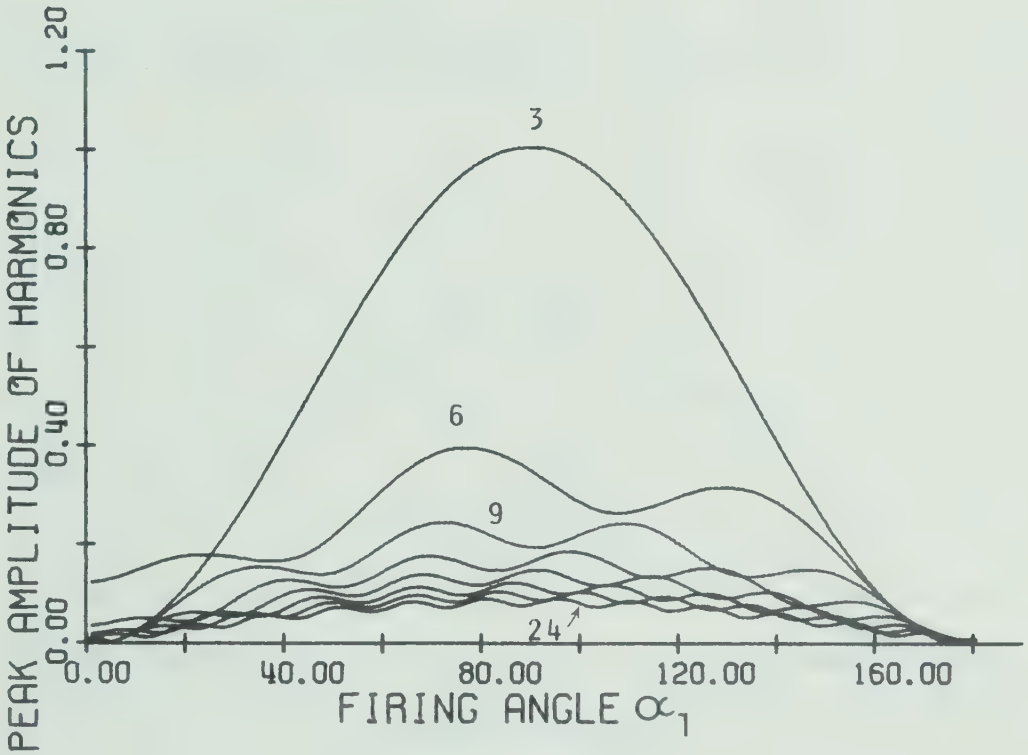


Fig. 3.19 Harmonic content in d.c. terminal voltage using the new control for α_2=5°, α_1=0-180°

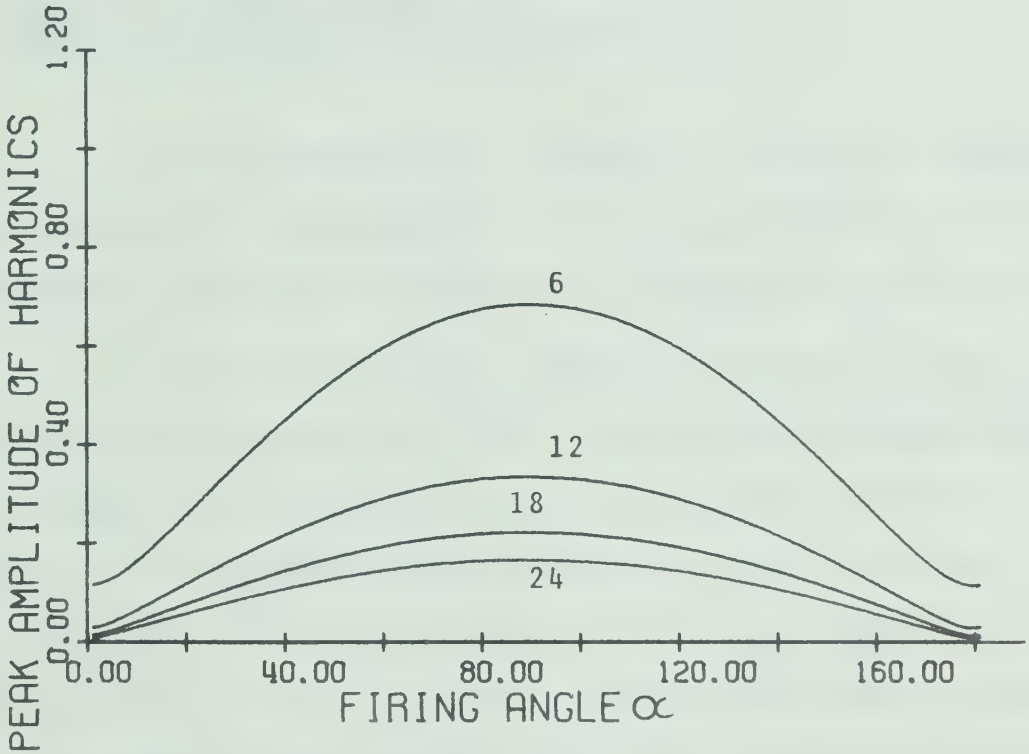


Fig. 3.20 Harmonic content in d.c. terminal voltage using conventional control

voltage for a converter using the new control, are higher than those for a converter using conventional control. This is of course at a certain d.c. voltage ratio

$$r = \frac{\text{Mean d.c. terminal voltage}}{\text{Maximum possible mean d.c. terminal voltage}}.$$

2. For a desired value of output d.c. voltage as a normal operating point for the converter α_1 and α_2 could be chosen such that the harmonic contents in the output d.c. voltage are as small as possible.

3. For converters using conventional controls the zero output voltage is obtained only at $\alpha = 90°$. At this angle the harmonic contents are maximum. While zero output voltage for converters using the new control could be obtained with any values of α_1 and α_2 such that $\alpha_1 + \alpha_2 = 180°$. Choosing the minimum value of α_2 as small as possible and the maximum value of α_1 as high as possible, the harmonic contents for zero output voltage approaches zero. This is obvious from studying curves of Fig. 3.19 and also the output voltage waveforms of Fig. 3.9 at which $\alpha_1 = 120$, $\alpha_2 = 60°$ and those of Fig. 3.12 at which $\alpha_1 = 150°$, $\alpha_2 = 30°$.

3.2.8 Reduction Of Reactive Loading Of The Supply By Using The New Control

The curves of Fig. 3.21 show the relationship between the d.c. terminal ratio r, and the normalized in-phase and quadrature components of current at the input I_P, and I_Q' respectively. Where:

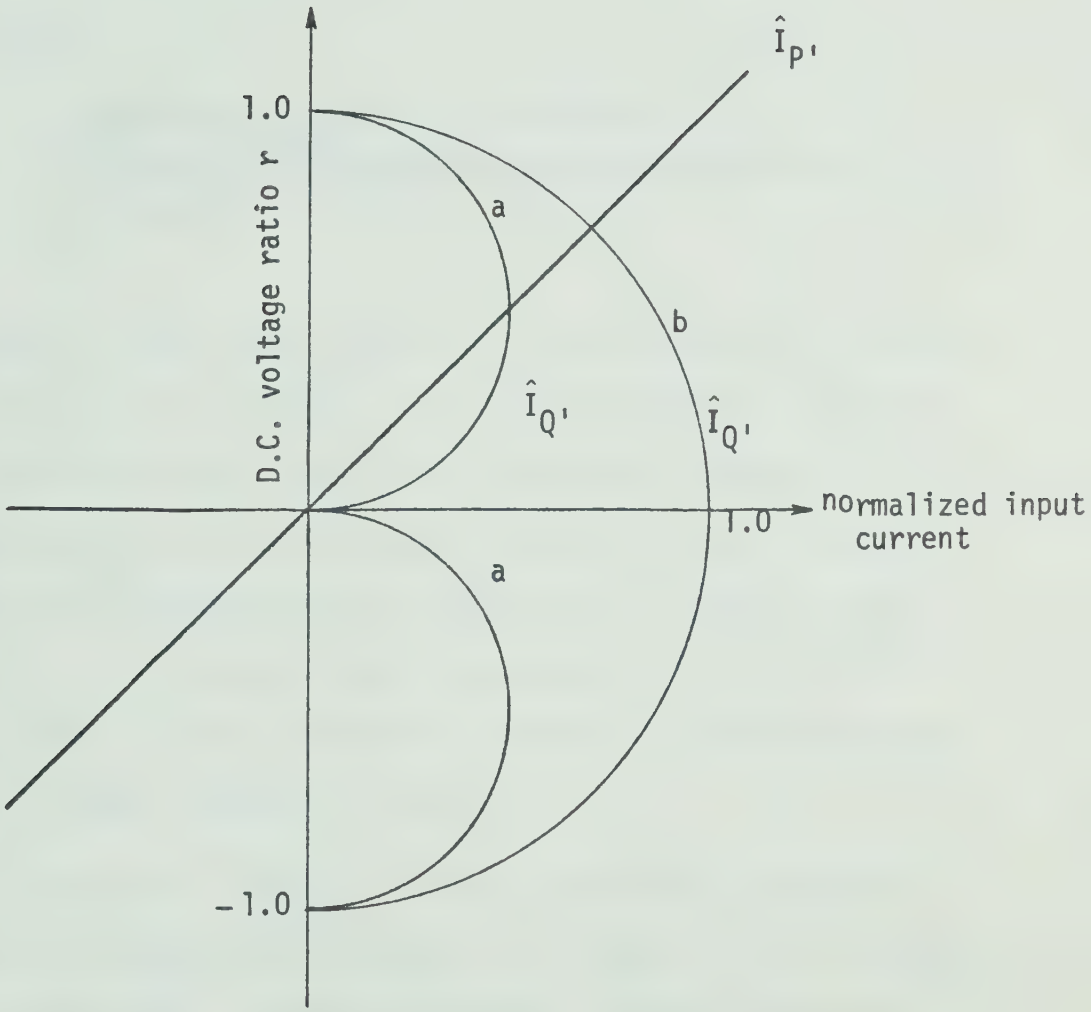


Fig. 3.2 1 Relationship between the d.c. terminal voltage ratio r, and the normalized components of input current for:

(a) Consecutive firing angle control

(b) Concurrent firing angle control

$$r = \frac{\text{Mean d.c. terminal voltage at firing angles } \alpha_1 \text{ and } \alpha_2}{\text{Maximum possible mean d.c. terminal voltage}}$$

$$= \cos \alpha_1 + \cos \alpha_2$$

$$\text{and } I_{P'} \text{ or } I_{Q'} = \frac{\text{amplitude of input current component with } I_d \text{ at output}}{\text{amplitude of fundamental input current with r=1, } I_d \text{ at output}}$$

Curve (a) shows this relation for a 6-pulse converter using a consecutive firing angle technique, as in the new control. Curve (b) shows the same relation with concurrent firing angle technique as in conventional controls. For both controls, the same linear relationship exists between the normalized in-phase component of current and the d.c. voltage ratio. For a converter using a consecutive firing angle technique, the maximum quadrature component of current is only half of that of a converter using a concurrent control.

At zero output voltage, a converter following a consecutive mode of operation consumes no fundamental input current, and consequently no mean a.c. input power. On the other hand a converter using conventional control consumes its maximum normalized quadrature current. Thus, so far as the the loading of the supply at reduced voltage ratio is concerned, the consecutive firing angle technique gives a converter considerably superior characteristics compared to another converter using conventional control. This is of great importance in many applications of phase-controlled converters as in the case of high-voltage d.c. power transmission .

3.2.9 Operation Of The 6-Pulse Converter With Discontinuous Current[1],[8],[7]

It has been assumed so far that the current at the d.c. terminals of the converter is continuous and perfectly smooth. This assumption implies that the a.c. ripple currents in the d.c. circuit are negligible in comparison with the direct component. In practice, of course, this assumption is never entirely valid; and in fact, it may often be the case that the magnitude of the a.c. ripple current is comparable with the direct component. However so long as the peak instantaneous value of the a.c. ripple current is less than the direct component, so that the net current is always greater than zero, and thus the converter is kept in continuous conduction, then the d.c. terminal voltage waveform at any given firing angle is theoretically the same as with perfectly smooth current (sections 3.2.5 and 3.2.6).

On the other hand, if the peak instantaneous negative value of the a.c. ripple current should exceed the d.c. component, then, since the net current flow cannot reverse, the direct current waveform becomes discontinuous, and the d.c. terminal voltage waveform departs from that obtained with continuous conduction. Moreover, since the voltage waveform is changed, the mean value of this waveform is also changed, and the relationship between the firing angle and the mean d.c. terminal voltage is not the same as with continuous conduction.

In practice, the continuity of the load current waveform depends upon the nature of the d.c. load circuit, and it is possible for discontinuous conduction to occur either in the rectifying or inverting

region of operation. If the load at the d.c. terminals is purely passive, and is capable only of absorbing mean power, then the current waveform inevitabley becomes discontinuous as the firing angle is retarded towards 90°. In order to illustrate this, the operation of a 6-pulse converter with a passive series inductance-resistance load will be considered. From an examination of the d.c. terminal voltage waveform for a 6-pulse converter (Figs. 3.12-3.17), it is clear that if the firing angle lies between 0° and 60°, the instantaneous voltage at the d.c. terminals is at all times positive, and hence, over this range of firing angles, the current in a passive load of this type must necessarily be continuous. As the firing angle is retarded beyond this point, however, the voltage at the d.c. terminals swings into the negative direction for certain periods of time, and it now depends upon the time constant of the load whether or not this negative voltage excursion can be absorbed, while a net positive current flow is maintained.

In Fig. 3.22, typical d.c. terminal voltage and current waveforms obtained at various firing angles, for series inductance-resistance loads having various time constants, are shown. At a, the load time constant is very large, and in this case, the current waveform remains continuous up to a firing angle only slightly in advance of 90°. The output voltage waveforms up to this point are the same as those obtained in section 3.2.6. At $\alpha = 90°$, the current has just become discontinuous, and there a short period during which there is no voltage or current at the d.c. terminals of the converter. It can be seen that

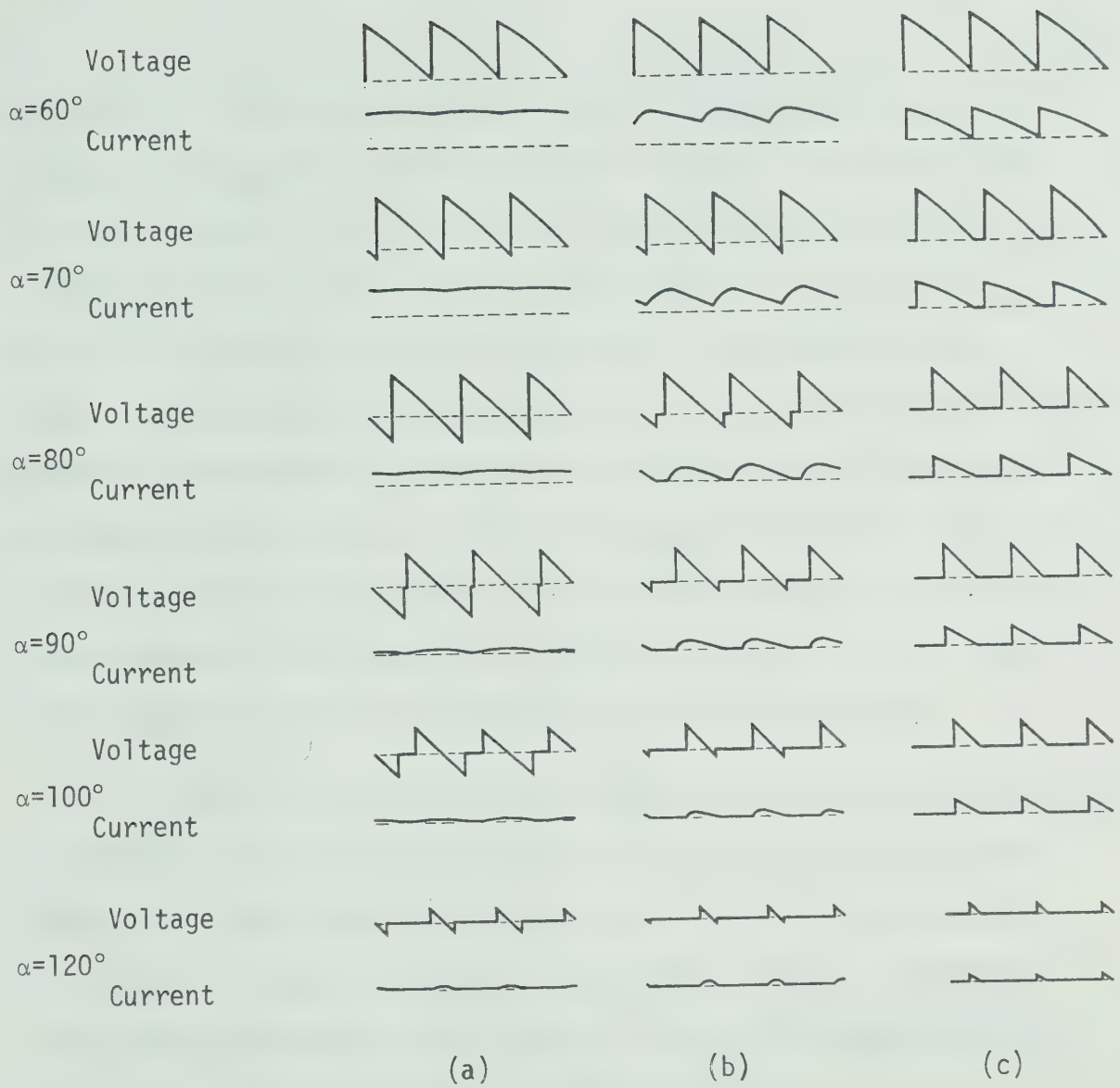


Fig. 3.22 D.C. terminal voltage and current waveforms obtained for a 6-pulse converter, with a series L-R load.

(a) $Q \to \infty$ (b) $Q=3$, (c) $Q=0$ (purely resistive)

$$Q = \frac{2\pi 6 f_i L}{R}, \quad f_i = \text{input frequency}$$

the effect of the zero-current period is to remove a small area of negative voltage which, with continuous conduction, would otherwise have been present, and hence the mean value of the d.c. terminal voltage is not quite zero, but slightly positive, say 0.5% of V_{dmax}. As the firing angle is retarded beyond 90°, the current waveform becomes more and more discontinuous, and the mean d.c. terminal voltage approaches zero more and more closely. Finally, at α = 120°, there is no conduction, and the d.c. terminal voltage becomes zero. Thus, with this load, within the region of discontinuous conduction, a relatively large movement of the converter firing angle results in only a very small change in the value of the mean d.c. terminal voltage.

Examining now the waveforms shown at b, which are appropriate to a load Q factor of about 3(at $6f_i$), it is seen that the current waveform has just become discontinuous at α = 80°. Once again, the d.c. terminal voltage becomes zero at α = 120°. At any intermediate firing angle, the mean value of the d.c. terminal voltage waveform is greater than that obtained with the higher Q load.

Finally, at c the waveforms are shown for a purely resistive load. In this case, it is clear that the conduction becomes discontinuous at α = 60°, and, once again, the d.c. terminal voltage becomes zero at α = 120°. At any intermediate firing angle, the mean value of the d.c. terminal voltage waveform is greater than at either a or b.

With loads which have the capability for storing voltage, for example a capacitor, or the armature of a d.c. machine with an induced

back emf, it is possible to obtain operation with discontinuous current at any point within the operating range, if the average load current demand is sufficiently small.

3.3 Control Techniques

3.3.1 Pulse Timing Principle

The control used is based on the principle of pulse timing control that has been referred to as the Commutating Voltage Integral Control Method. The application of this control principle in the inversion range will be given in detail. Then an extension of this control to cover the whole range will be discussed.

3.3.2 Invertor Control Criteria[3],[5],[6]

The criterion for the safe invertor operation is that the angle of advance β must be large enough so that the extinction angle δ left at the end of commutation is not less than δ_o, the deionization time of the valve which has just stopped conducting. The practical value of δ_o is very small (in the order of 1° to 2°), and the control circuits would generally be designed to maintain δ to a constant value of δ_c (with practical values of 5° to 10°). The ensuing control is referred to as constant extinction angle control (CEA).

3.3.3 Equations of CEA Control

As shown in Appendix I, under steady-state condition and assuming sinusoidal waveforms, the equation which defines the commutating process in a 3-phase bridge circuit is well known:

$$\sqrt{2} \times \hat{V}_N \cos \beta_1 - \sqrt{2} \times \hat{V}_N \cos \delta_1 + 2\omega L I_d = 0 \qquad (3.29)$$

Where β_1 and δ_1 referred to any valve of the upper valves in the bridge. The commutating reactance $2\omega L$ is mainly the reactance of two convertor transformer phases, and assumed constant. $\hat{V}_N$ is the rms value of the commutating voltage of the particular valve.

For commutation among the lower valves, the equation corresponding to equations (3.29) is,

$$\sqrt{2} \times \hat{V}_N \cos \beta_2 - \sqrt{2} \times \hat{V}_N \cos \delta_2 + 2\omega L I_d = 0 \qquad (3.30)$$

The control used should ensure that during inverter operation the angle of delay $\alpha_2 = \pi - \beta_2$, does not become so large as to cause an overlap of the commutation periods of the lower valves with the firing points of the upper valves. Otherwise the extinction angle obtained for the upper or both upper and lower valves will be reduced below the computed value and may result in commutation failure.

For CEA control we put $\delta_1 = \delta_c$ in equation (3.29)

$$\sqrt{2}\, \hat{V}_N \cos \beta_1 - \sqrt{2}\, \hat{V}_N \cos \delta_c + 2\omega L I_d = 0 \qquad (3.31)$$

To prevent the angle of advance β_2 of the lower valves from falling below the minimum required value of $\beta_1 + \mu_2$, δ_2 of equations (3.30) should be equal to β_1 of equation (3.31) and equation (3.30) becomes,

$$\sqrt{2}\, V_N \cos \beta_2 - \sqrt{2}\, V_N \cos \beta_1 + 2\omega L I_d = 0 \qquad (3.32)$$

substituting $\cos \beta_1$ from equation (3.31) into equation (3.32) gives,

$$\sqrt{2}\, \hat{V}_N \cos \beta_2 - \sqrt{2}\, \hat{V}_N \cos \delta_c + 4\omega L I_d = 0 \qquad (3.33)$$

Now substituting $\omega t = \pi - \beta_1$, equation (3.31) for the upper valves gives,

$$\sqrt{2}\, \hat{V}_N \cos \omega t + \sqrt{2}\, \hat{V}_N \cos \delta_c - 2\omega L I_d = 0 \qquad (3.34)$$

Similarly, for the lower valves substituting $\omega t = \pi - \beta_2$, equation (3.33) becomes,

$$\sqrt{2}\, \hat{V}_N \cos \omega t + \sqrt{2}\, \hat{V}_N \cos \delta_c - 4\omega L I_d = 0 \qquad (3.35)$$

Thus for CEA control, correct firing angles for the upper and lower values will be given when equations (3.34) and (3.35) are satisfied. The extra amplitude $2\omega L I_d$ in equation (3.35) accounts for the larger firing angle required for lower values.

3.3.4 Applying The Pulse Timing Principle For CEA Control

The principle is based upon the integration of the commutation voltage for the corresponding valve. Since equations (3.34), (3.35) are the basic equations to be satisfied, it is more convenient to write them in the form:

$$-\sqrt{2}\,\hat{V}_N \cos \omega t - \sqrt{2}\,\hat{V}_N \cos \delta_c + 2\omega L I_d = 0 \qquad (3.36)$$

$$-\sqrt{2}\,\hat{V}_N \cos \omega t - \sqrt{2}\,\hat{V}_N \cos \delta_c + 4\omega L I_d = 0 \qquad (3.37)$$

to represent the commutation process in the upper and lower valves respectively.

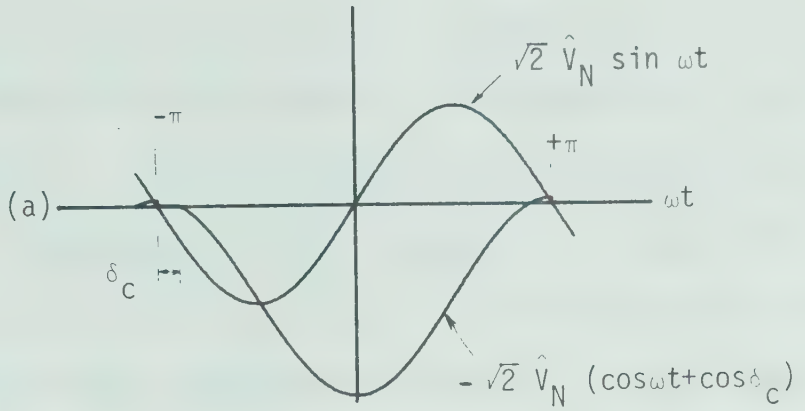
Considering first the upper valves, the first two terms in equation (3.36) are generated by integration of the commutation voltage waveform $e = \sqrt{2} \times \hat{V}_N \sin \omega t$ from $-\pi + \delta_c$ as shown in Fig. 3.23(a)

$$\text{Integral } I = \int_{-\pi+\delta_c}^{\omega t} \sqrt{2}\,\hat{V}_N \sin \omega t \, d\omega t$$

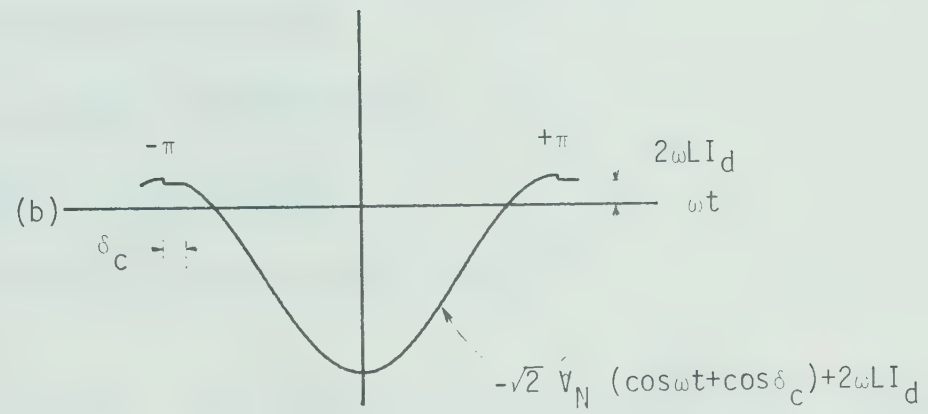
$$= -\sqrt{2}\,\hat{V}_N \cos \omega t - \sqrt{2}\,\hat{V}_N \cos \delta_c \qquad (3.38)$$

The output of the integrator goes negative, reaching its peak of $-\sqrt{2} \times \hat{V}_N (1 + \cos \delta_c)$ at $\omega t = 0$; coming back to zero at $\omega t = \pi - \delta_c$, then goes positive. At the next zero voltage the integration is clamped to zero for a fresh start of the integration for the next cycle. Clearly the computation is carried out afresh each cycle and there is no memory of the voltage during previous cycles. The circuit therefore is capable of readjusting itself on a cycle-to-cycle basis.

The remaining term, $2\omega L I_d$ is easily obtained by passing the current I_d through a resistance equal to $2\omega L$. By adding this term to the integral I a resultant waveform R_1 is produced as shown in Fig. 3.23(b),



(a)



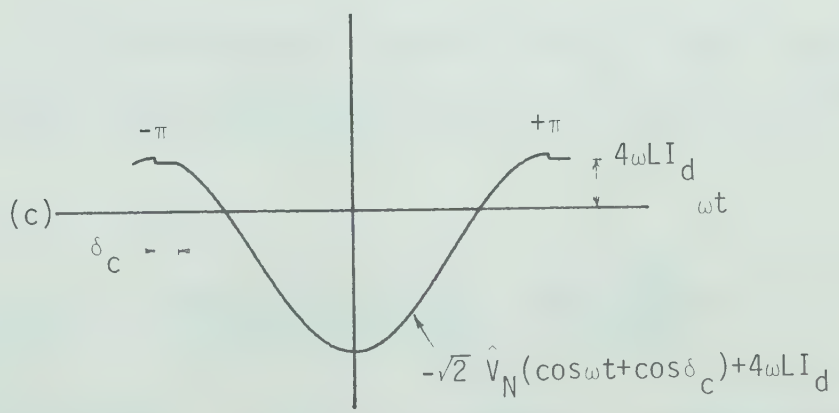


Fig. 3.23 (a) Clamped integrator output waveform

(b) CEA output waveform for valve 1 (upper valves)

(c) CEA output waveform for valve 2 (lower valves)

the point at which this waveform passes through zero in a positve going direction, gives the angle of advance β_1 for upper valve 1, say.

Similarly a resultant waveform R_2 could be obtained for the lower valves by adding $4\omega L I_d$ to the integral I as shown in Fig. 3.23(c). Here the point at which this waveform passes through zero in the positive direction gives the angle of advance β_2 for the lower valve 4, say. In a similar manner the resultant waveforms of other valves in the two groups could be obtained.

3.3.5 Transient Response Of CEA Control

3.3.5.1 Changes In Direct Current

The simulated equation would then be:

$$\sqrt{2}\,\hat{V}_N \cos\beta - \sqrt{2} \times \hat{V}_N \cos\delta_c + 2\omega L I_d + L' \frac{dI_d}{dt} = 0 \qquad (3.39)$$

If it is assumed that the rate of change of direct current dI_d/dt remains the same during commutation, the commutation equation is from (3.39).

$$\sqrt{2}\,\hat{V}_N \cos\beta - \sqrt{2}\,\hat{V}_N \cos\delta_c + 2\omega L I_d + 2\omega L \frac{\mu}{\omega} \frac{dI_d}{dt} = 0 \qquad (3.40)$$

Thus the required value $L' = 2\omega L\ (\mu/\omega)$. However, μ is not known and theoretically the safest value to take would be the maximum expected value of μ, say $\pi/6$ to $\pi/5$. Under normal steady-state operating conditions the rate of change of current caused by ripple would be negligible

Significant changes would occur during changes in current settings and worst conditions may be expected when one of the invertor bridges is blocked or has a commutation failure. In this case the rate of rise of current may be in excess of 10^5 Amp./Sec.

3.3.5.2 Changes In A.C. Voltages

The new control described in the foregoing is based on the simulation of the steady-state equation, implying a sinusoidal a.c. voltage, and is so devised as to provide independent computation for each cycle. This control therefore provides an effective and rapid adjustment to new conditions. It is however important that if there are sudden voltage changes during a particular cycle it should not result in commutation failure.

Examination of the waveforms in Fig. 3.2 4(a) shows that if, say, due to a fault somewhere in the a.c. system a sudden fall occurs in the a.c. voltage, this will result in the positive voltage integral being less than the negative integral, leading to a consequent reduction of δ_c. If the voltage reduction is large, this may well result in the pulse not arriving at all. It would therefore be appropriate to cope with transient conditions by detecting such changes and providing an increase in the angle of advance.

It may be noted from Fig. 3.24(b) that when the a.c. fault is removed, the a.c. voltage will rise and result in an increased δ. No compensating action is therefore necessary.

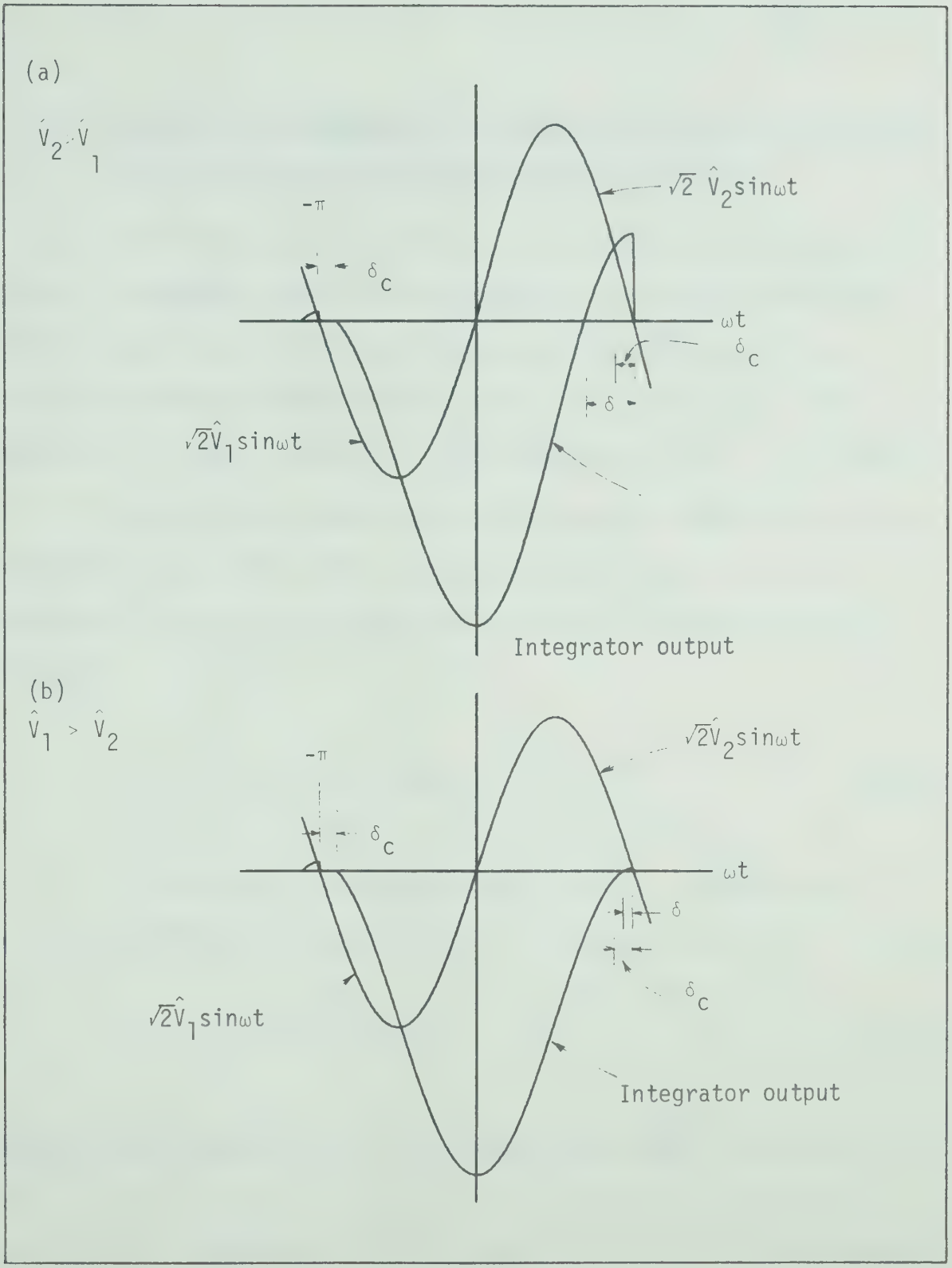


Fig. 3.24 CEA control output voltage waveforms for transient conditions on ac system

3.3.5.3 Detection And Compensation For Sudden Changes In A.C. Voltages

Principle Of Commutating Voltage Waveform Analyzer

Referring to Fig. 3.23, it is seen that with the proposed control arrangement there are two continuously available voltage waveforms, namely the commutating voltage waveform ($\sqrt{2}\ \hat{V}_N \sin \omega t$) and integrator output waveform ($-\sqrt{2}\ \hat{V}_N \cos \omega t - \sqrt{2}\ \hat{V}_N \cos \delta_c$). These waveforms are used to detect the transient change in the a.c. voltage.

Examination of the integrator output and commutating voltage waveforms reveals that under steady-state conditions, the direct summation of these two waveforms will produce a resultant waveform S given by

$$S = \sqrt{2}\ \hat{V}_N \ [\sin \omega t - \cos \omega t - \cos \delta_c] \tag{3.41}$$

This waveform will pass through the zero reference level in a positive direction at ωt given by:

$$\omega t = \frac{1}{2} \text{ arc sin } (\sin^2 \delta_c) \tag{3.42}$$

and for small values of δ_c i.e. $\delta_c \leq 20°$, this point is given by:

$$\omega t \doteq \frac{\pi}{2} \tag{3.43}$$

For transients which result in a reduced positive voltage integral of the commutating voltage, the summation waveform S will pass

through zero at some point after $\omega t = \pi/2$. Therefore the point at which the summation waveform S passes through zero in a positive going direction may be detected and if this point does not arrive at or before $\pi/2$, some transient compensation is necessary. It may be noted that this method analyzes the waveform between the limits $\omega t = -\pi$ and $\omega t = -\frac{\pi}{2}$. Thus, in this case it would be too late if a fault occured after $\omega t = \frac{\pi}{2}$. It is however possible to shift the zero crossing of the summation waveform S by feeding in a fraction K of the sine function which gives:

$$S = \sqrt{2}\,\hat{V}_N\,(K \sin \omega t - \cos \omega t - \cos \delta_c) \qquad (3.44)$$

Inspection of (3.44) reveals that under steady-state conditions, if K is reduced from unity to zero, the summation waveform S crosses zero between $\omega t = \pi/2$ to $\omega t = \pi - \delta_c$.

It is obvious, however, that detection must be made sufficiently early to allow for any compensation and on the other hand, the maximum possible part of the cycle should be covered. Assuming that the maximum required angle of advance for CEA control under steady-state conditions is unlikely to be greater than 150°, the detection may be best carried out up to $\omega t = 120°$, thus allowing for a compensation β of 60°.

If $S = 0$ at $\omega t = \frac{2\pi}{3}$, then

$$K = [\cos \delta_c + \cos \frac{2\pi}{3}]/\sin \frac{2\pi}{3} \qquad (3.45)$$

and for $\delta_c = 10°$

$$K = 0.56$$

It should be noted that under steady conditions, the point at which the summation waveform S passes through zero in a positive going direction is independent of the peak magnitude of the a.c. voltage.

The question arises as to what action should be taken subsequent to the detection. It would seem best to provide the firing signal at the point of detection. For example, if for the transient detector set for 120°, zero crossing does not occur before 120° then a firing pulse should be given immediately. This may result in some over compensation, in some cases. This would not be detremental since the control system is capable of fresh computation each cycle.

3.3.6 Control Over The Remaining Range Of Converter Operation

3.3.6.1 Introduction:

As in conventional controls a method is required for compounding the converter over the remaining range of converter operation. The object being to maintain a certain controlled parameter for the control of the firing angle and therefore voltage over the available range.

In conventional controls we need only one controlled parameter since the firing angle is the same for all valves. In the new control we need two controlled parameters, one for each group.

3.3.6.2 Principle

If a positive voltage level V_{c_1} is added to the CEA summation waveform of Fig. 3.23(b) for the upper valves, the summation waveform R_1 becomes,

$$R_1 = -\sqrt{2}\, V_N (\cos \omega t + \cos \delta_c) + 2\omega L I_d + V_{c_1} \qquad (3.46)$$

and is shown in Fig. 3.25(a), the angle of advance β_1 is given where R_1 goes through zero in a positive going direction. In fact it is now greater than that required for CEA control.

Similarly if a positive voltage level V_{c_1} is added to the CEA summation waveform of Fig. 3.23(c) for the lower valves, R_2 becomes:

$$R_2 = -\sqrt{2}\, V_N (\cos \omega t + \cos \delta_c) + 4\omega L I_d + V_{c_2} \qquad (3.47)$$

as shown in Fig. 3.25(b) the angle of advance β_2 is given in the same manner as the angle of advance β_1.

Clearly, when both V_{c_1} and V_{c_2} are equal to zero, the two groups of the converter will operate on CEA control. As V_{c_2} is increased above zero with $V_{c_1} = 0$, the upper valves will continue to operate on

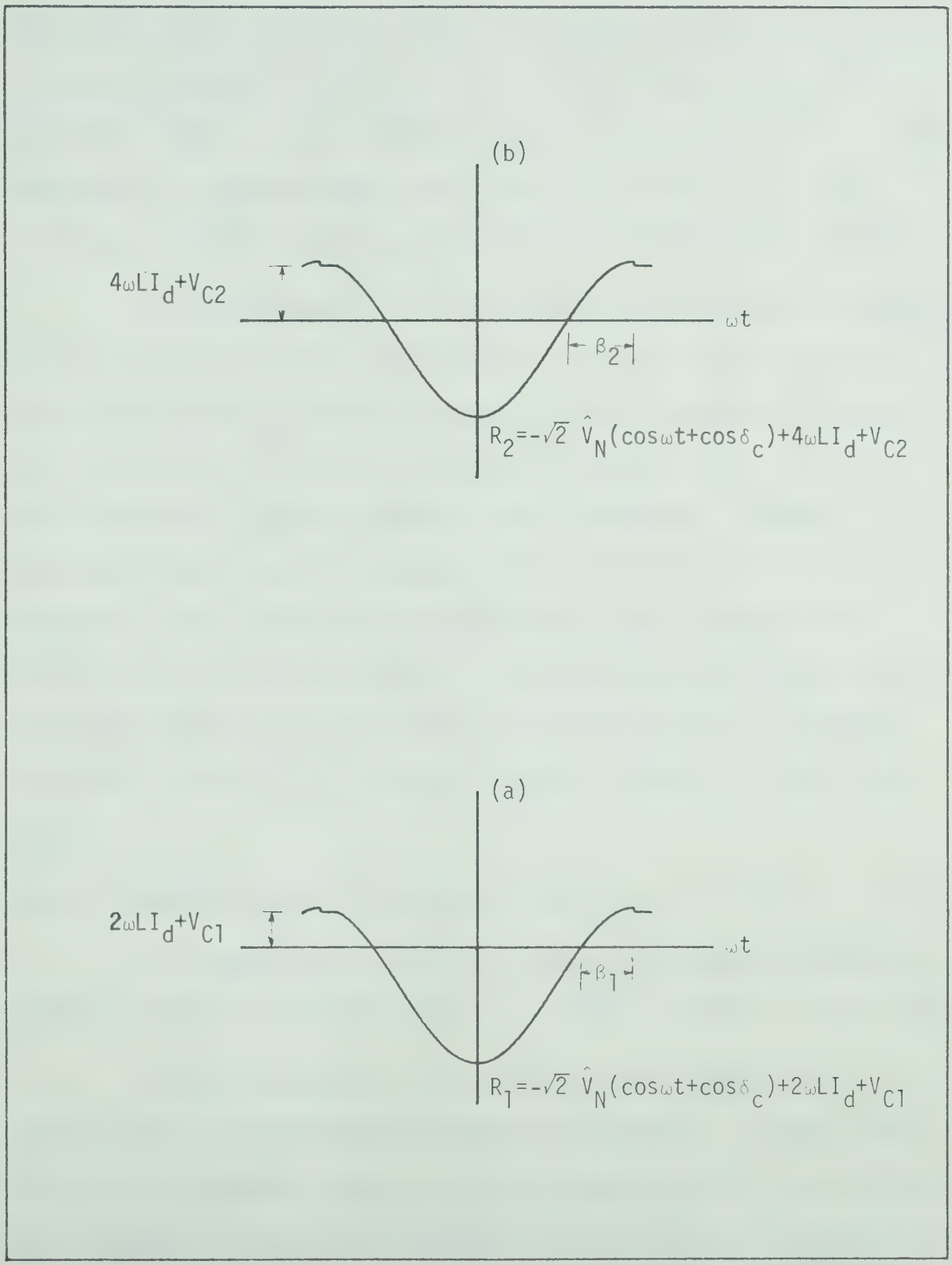


Fig. 3.25 Combined CEA control with rectification control

(a) for upper valves

(b) for lower valves

CEA control while the lower valves will operate at some angle of advance β_2 given by equation (3.47) for this particular value of V_{c_2}. The converter output voltage is reduced. As V_{c_2} is increased to its maximum value which is greater than or equal to $\sqrt{2}\,\hat{V}_N\,(1 + \cos\delta_c) - 4\omega L I_d$, the lower valves will continue to operate at minimum angle of delay α_c.

If the voltage V_{c_1} is now increased above zero to its maximum required value of greater than or equal to $\sqrt{2}\,\hat{V}_N\,(1 + \cos\delta_c) - 2\omega L I_d$, with the voltage V_{c_2} held at its maximum value, the angle of advance β_1 of the upper valves will be increased to greater than that required for CEA control. And the converter output voltage will become increasingly positive. Thus the converter has now entered into rectifier operation. As V_{c_1} attains its maximum value, both upper and lower valves in the bridge will operate at a minimum angle of delay α_c resulting in maximum rectifier output voltage, Thus the converter is operated following a"consecutive firing angle control technique" as mentioned before.

3.3.6.3 Technique Used For Providing V_{c_1} and V_{c_2}

In conventional control, V_{c_1} and V_{c_2} are obtained through a feed-back loop. The control signal is a current, voltage or power signal.

In the new control in which the control signal is an external one, the relationships between the output d.c. voltage (mean value) and the external signal, could be adjusted to suit any required form and shape. Accordingly a method for providing V_{c_1} and V_{c_2} could be designed.

To illustrate this, let the required control characteristics be as shown in Fig. 3.26 which could be written as:

$$V_d = V_{dmax}^{+} \qquad e > e_2 \tag{3.48}$$

$$V_d = A_1 e \qquad e_2 > e > e_1 \tag{3.49}$$

$$V_d = - A_2 e \qquad e_1 > e > o \tag{3.50}$$

$$V_d = - V_{dmax}^{-} \qquad e < o \tag{3.51}$$

where V_d is the steady d.c. component of the output voltage, e is the external control signal, A_1 and A_2 are constants that could be made equal. V_{dmax}^{+} and V_{dmax}^{-} are the positive and negative ceiling voltages.

To achieve this characteristic, a requirement of the controller which provides V_{c_1} associated with the upper valves, is that the output of this controller should be zero when the output V_{c_2} from the other controller is less than its maximum value required for operation of the lower valves at the minimum angle of delay α_c.

This controller should also ensure that V_{c_1} is held at its maximum value after reaching it.

A requirement of the controller which provides V_{c_2} associated with the lower valves is that the output of this controller be held at the maximum required value for operation of the lower valves at a min-

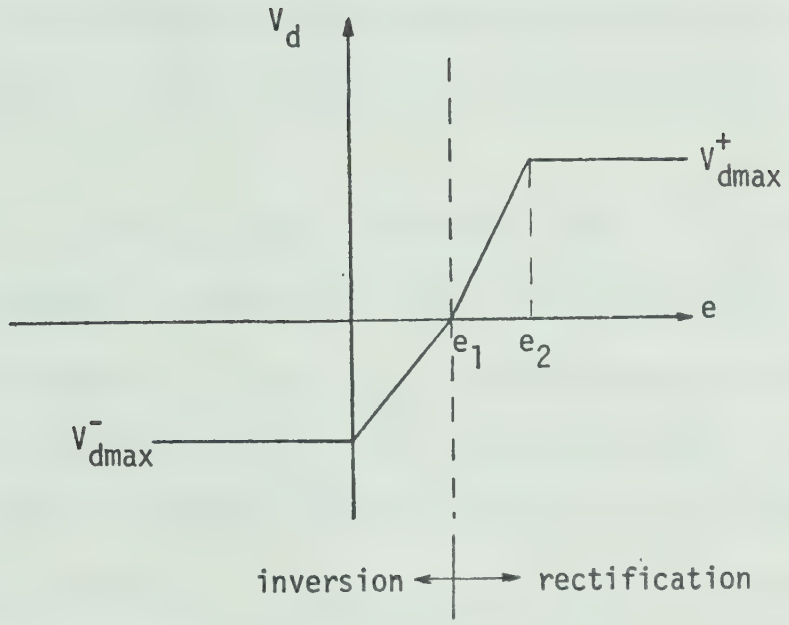


Fig. 3.26 Control characteristic over the whole range of converter

imum angle of delay α_c when V_{c_1} is other than zero. The two controllers should be designed so that their outputs are prevented from going negative.

Fig. 3.27 (a) and (b) show the required relations between the external signal and V_{c_1} and V_{c_2} respectively, that will satisfy these requirements.

For $e > o$ both V_{c_1} and V_{c_2} are equal to zero. The two groups and hence the converter are operating at full inversion on CEA control.

In the region $o < e < e_1$, $V_{c_1} = o$ and the upper group will be still operating on CEA control. V_{c_2} will have a value other than zero and the lower group will operate from full inversion to full rectification.

For the period $e_1 < e < e_2$, V_{c_2} will be held at its maximum value, and the lower group will be still operating at full rectification. V_{c_1} will have a value rather than zero, and the lower group will be operating from full inversion to full rectification. For any value of e such that $e > e_1$ both groups will be operating at full rectification.

Thus this technique leads to the consecutive mode of operation of the converter described before.

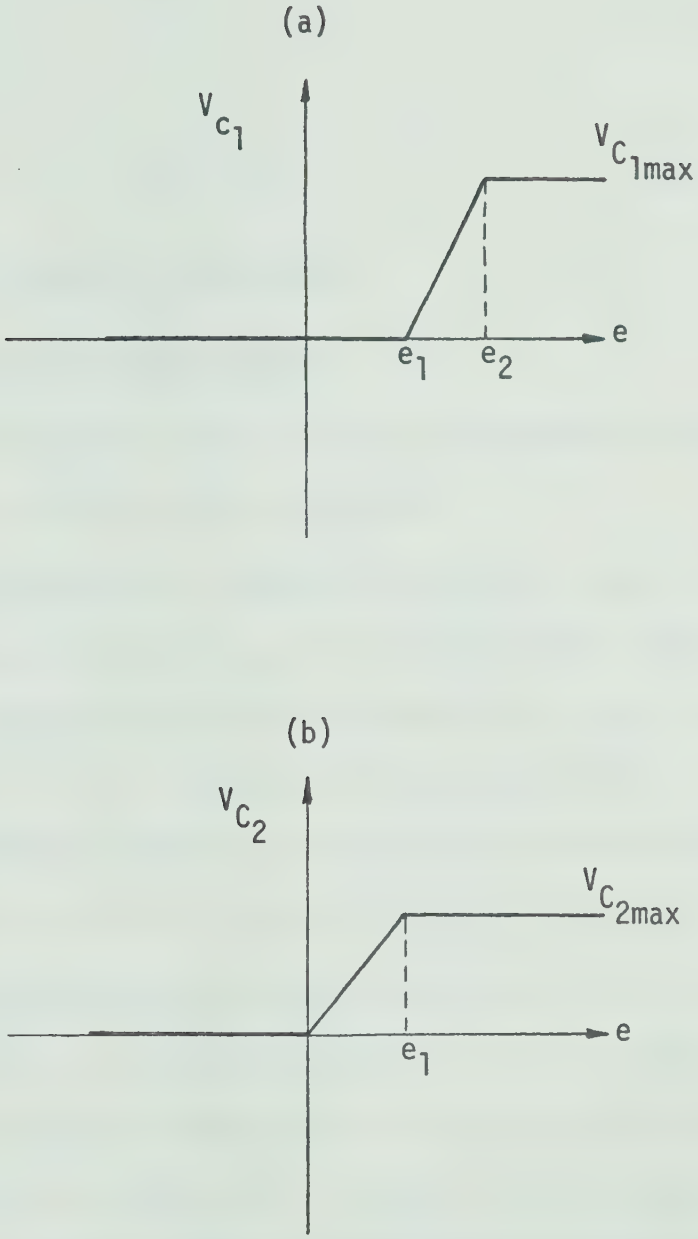


Fig. 3.27 Relationship between the external signal e and V_{C_1}, V_{C_2}

CHAPTER IV

PRACTICAL ARRANGEMENT

4.1 Block Diagram of The Control System

The block diagram of the practical arrangement is shown in fig. 4.1, which is generally self-explanatory.

The level detector A, detects the positive going zeros of the commutating voltage waveform $\sqrt{2}\ \hat{V}_N \sin \omega t$ and provides a trigger at such points. These trigger pulses operate the monostable circuit with the set operating time $T = \delta_c$. Operation of the monostable circuit opens the gate for operation of the zero clamping circuit which discharges the integrator output and clamps it to zero for the period $T = \delta_c$.

This integrator output and the signal $2\omega LI_d$ ($4\omega LI_d$ for the lower valves) are fed into the level detector B, which detects the instant when the summation signal passes through zero while going positive. The trigger from the level detector is used as the starting point of the firing pulse. fig. 4.2 shows the integrator arrangement along with its connections to the clamping circuit[9]. A FET is used here as a switch. The control signal (output of the monostable circuit) is applied between gate and source of the FET. At time $\omega t = -\pi$ the FET is switched on, the integrator discharges to zero with a time constant determined by the size of the capacitor and the saturation resistance of the FET. After a period of δ_c, the FET is switched off, and integration

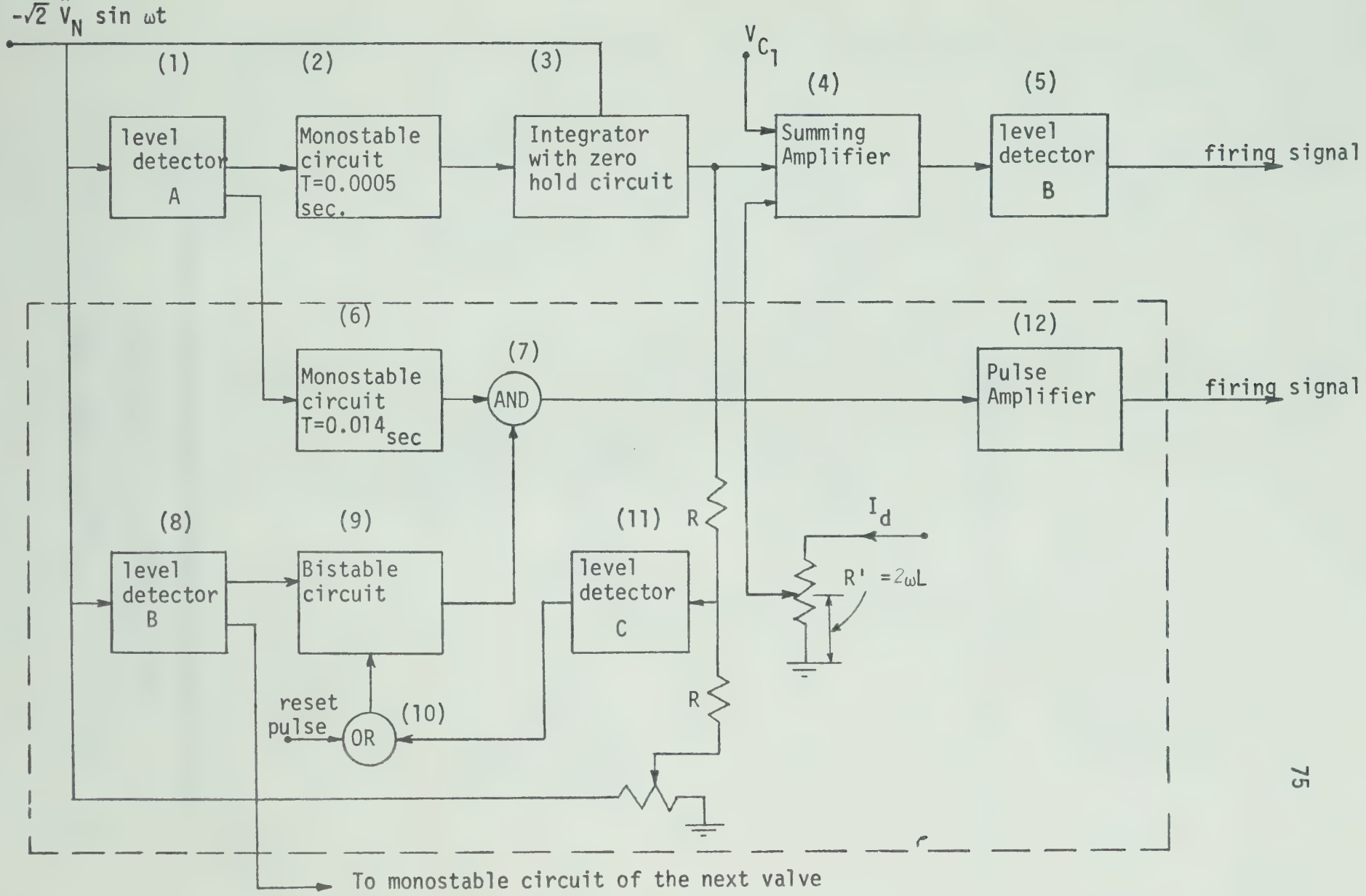


Fig. 4.1 Block diagram of the control system for one valve

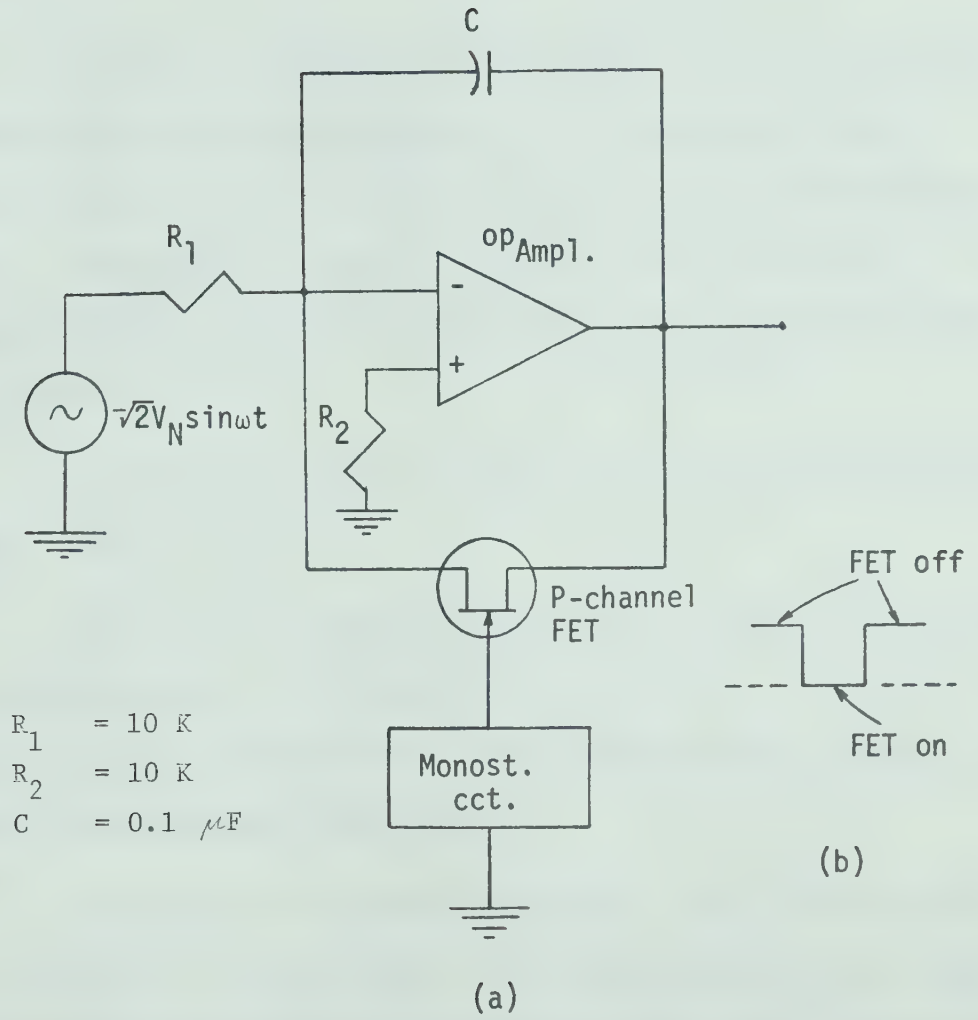


Fig. 4.2(a) The integrator arrangement along with its connection to the clamping circuit

Fig. 4.2(b) Input signal to FET

starts again. It has to be ensured that the feedback capacitor is fully discharged before the time $\omega t = - \pi + \delta_c$ i.e. the time constant for the discharge of c must be very much less than the minimum required value of δ_c.

The circuit arrangement inside the dotted lines, represents the commutating voltage wave analyzer. Level detector A gives a positive trigger at $\omega t = - \pi$ which is used to trigger the monostable circuit. The monostable circuit is set to operate up to 2°or 3° after the point when the summation waveform would cross zero under steady-state conditions.

The bistable circuit is reset by a trigger from level detector B at the instant $\omega t = o$.

The sum of the integrator output and $K \sqrt{2} \hat{V}_N \sin \omega t$, obtained from a potentiometer, is fed into a level detector C. The latter gives a trigger when the sum passes zero while going positive, and this trigger is used to operate the bistable circuit.

The output of the monostable circuit, and bistable circuit, Fig. 4.3(b) and (c) respectively, are fed into an AND gate. If the bistable circuit does not operate before the monostable circuit resets itself, then the AND gate would operate. The operation of the AND gate is used to provide a trigger for starting the pulse.

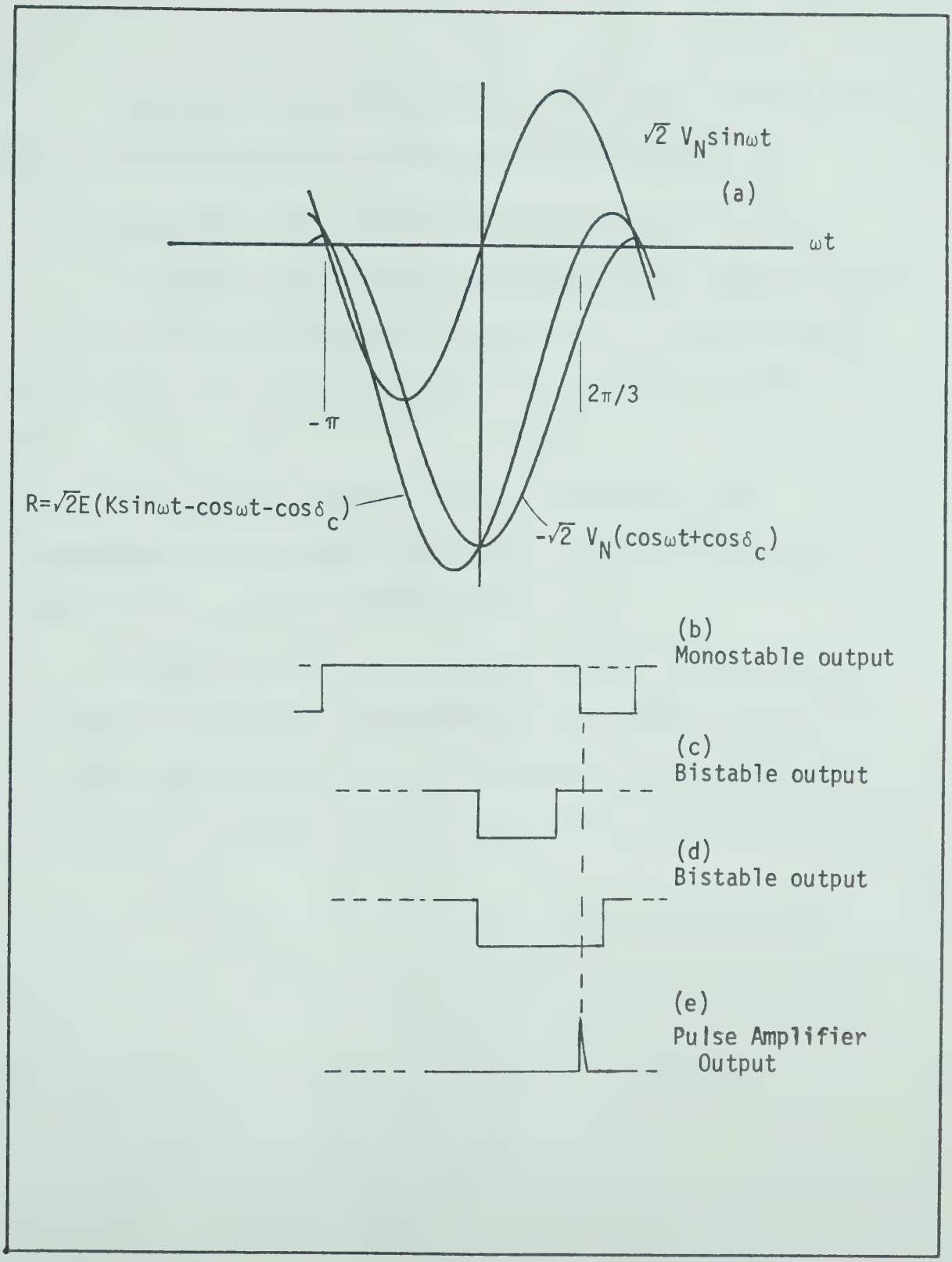


Fig. 4.3 Typical operation of commutating voltage waveform analyzer

Most of the circuits involved in the block diagram of fig. 4.1 are standard circuits and need not be described here.

4.2 Block diagram of the controllers providing V_{c1} and V_{c2}

The requirements of the controllers used to provide V_{c1} and V_{c2} had been discussed in the previous chapter. A block diagram of an arrangement which provides such a form of control is shown in fig. 4.4.

The control signal e is fed to amplifiers 1 and 2. The gate controlling the output of amplifier 1, is operated by a level sensor when V_{c2} reaches its maximum value.

Both amplifiers are chosen such that V_{c1} and V_{c2} are held at their maximum values, corresponding to the minimum angle of delay α_c, after reaching these values. The outputs of both amplifiers are prevented from going negative by diodes D_1 and D_2.

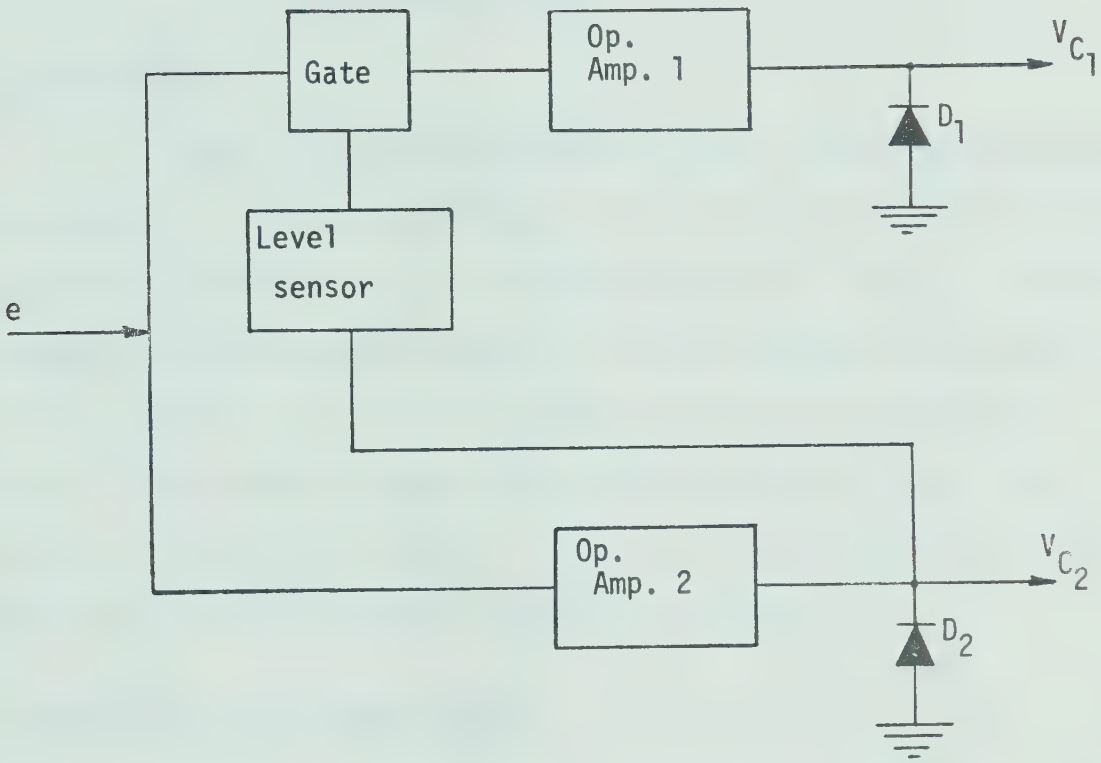


Fig. 4.4 Block diagram of the arrangement for providing V_{C_1} and V_{C_2}

CHAPTER V

EXPERIMENTAL RESULTS

5.1 Introduction

In order to test the performance of the control system described in this work, a 6-pulse converter was built, along with a control circuit to provide the firing pulses of the converter valves. Fig. 5.1 shows the details of the converter circuit. A block diagram of the control circuit is shown in Fig. 5.2. The control circuit is the same as in Fig. 4.1 except for the commutating voltage wave analyzer which was omitted, to simplify the system. This will not affect the test results since the a.c. supply provides a regulated voltage.

5.2 Components of the test circuit

Most of the components used in the control circuit are standard. Technical data appear in Appendix II. The converter bridge consists of 6 silicon controlled rectifiers, type 2N690. For ratings and triggering characteristics refer to Appendix III.

5.3 Test Results

5.3.1 Control Circuit Waveforms

Fig. 5.3 shows the output waveforms of the summation amplifiers for different values of V_c and hence different firing angles. These waveforms are shown along with the input sine waves to demonstrate the control principle.

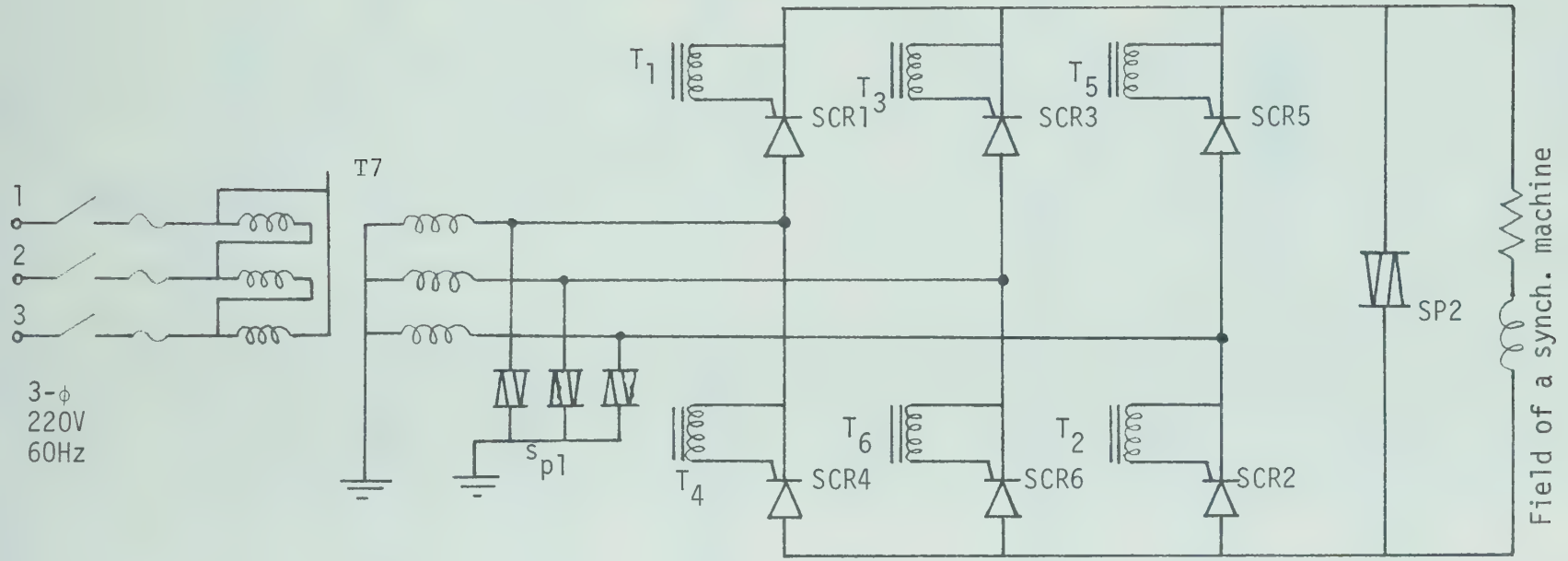


Fig. 5.1 Connection of the converter circuit for test

SCR1-6	Type 2N690 Thyristors
T1-6	Hammond transformer Type RL 147
SP1	3 Thyrectors for 120v r.m.s. operation
SP2	2 back-to-back A27C (GE) avalenche diodes 350-400 v.
T7	3-phase transformer 220/110 volts

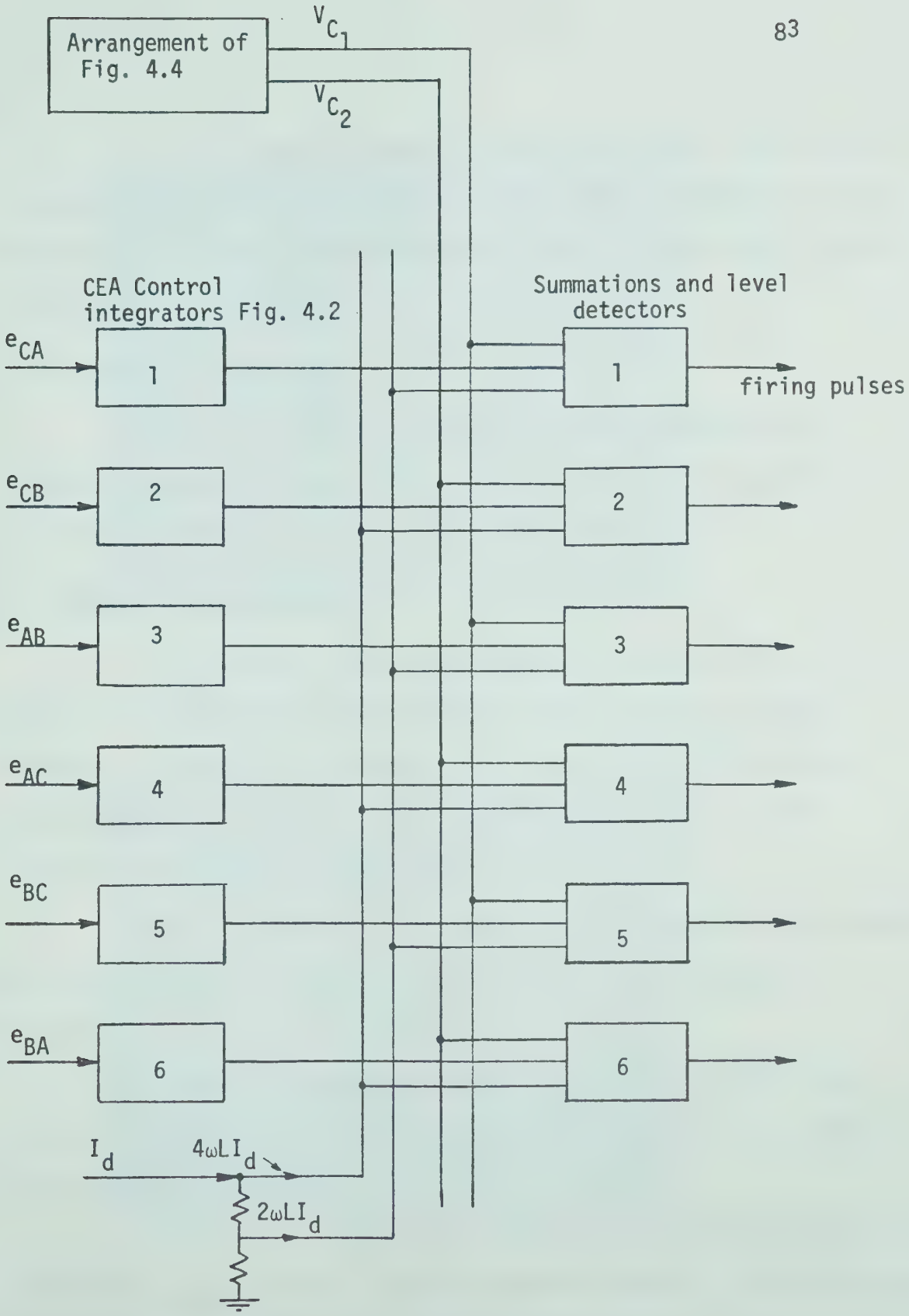


Fig. 5.2 Control circuit arrangements for test

Fig. 5.4 shows the output of level detectors B. This output represents the firing pulses to the valves. These waveforms are also shown along with the summation amplifier output to show clearly how the firing pulses are produced.

5.3.2 Output D.C. Waveforms

Figs. 5.5-11 show the output D.C. voltage waveforms for different values of firing angles α_1 and α_2. For instant comparison, theoretical waveforms are also shown, Figs. 5.12-5.19.

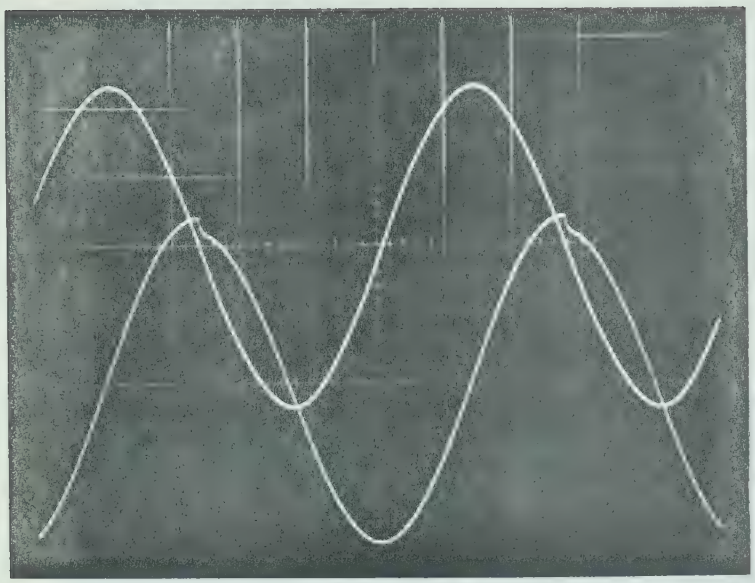
5.4 Comments On Test Results

1. The control circuit waveforms are similar to those obtained theoretically except that the integrator output is not discharged instantly. Actually the integrator discharges with a time constant which depends on the value of the discharging capacitor, and the saturation resistance of the FET used.

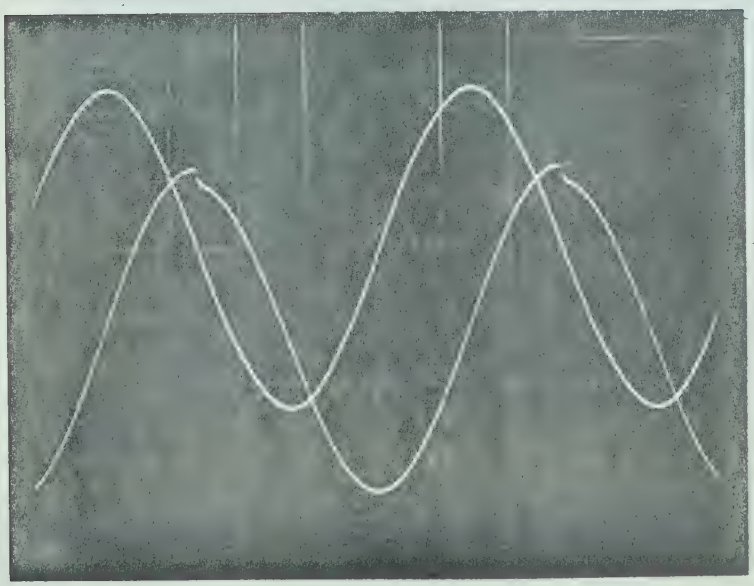
This of course will not affect the performance of the integrator as long as this time constant is less than δ_c. This is clear in Fig. 5.20.

2. The d.c. voltage waveforms obtained from the test are similar to those obtained theoretically for the region $\alpha_1+\alpha_2 \leq 180°$ i.e. in the rectification region.

3. The actual waveforms deviated from the theoretical ones for the region $\alpha_1+\alpha_2 > 180°$ i.e. for the inversion region. This is due to the nature of the load used. Refer to the discussion of the operation of the converter with discontinuous current in section 3.2.9.



(a)



(b)

Fig. 5.3 Output waveforms of summation amplifiers

(a) for $\alpha = \alpha_{max}$

(b) for $\alpha_{min} < \alpha < \alpha_{max}$

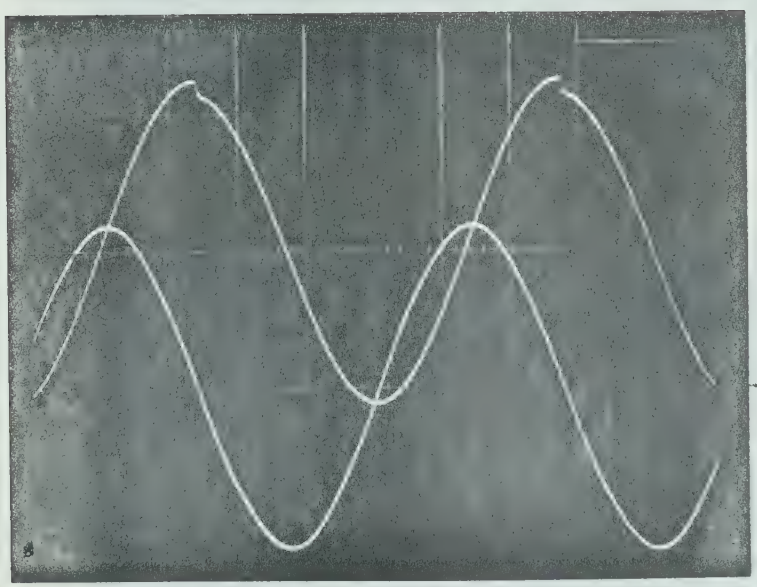
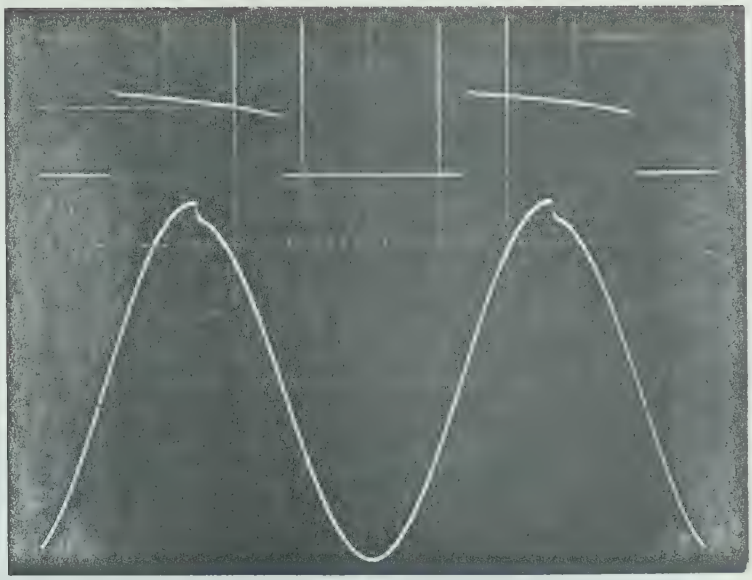


Fig. 5.3 (continued)
(c) for $\alpha=\alpha_{min}$

a



b

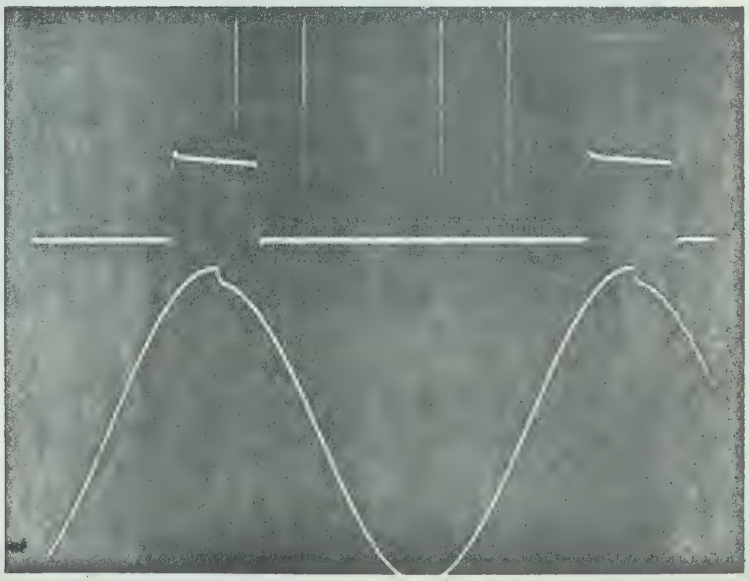
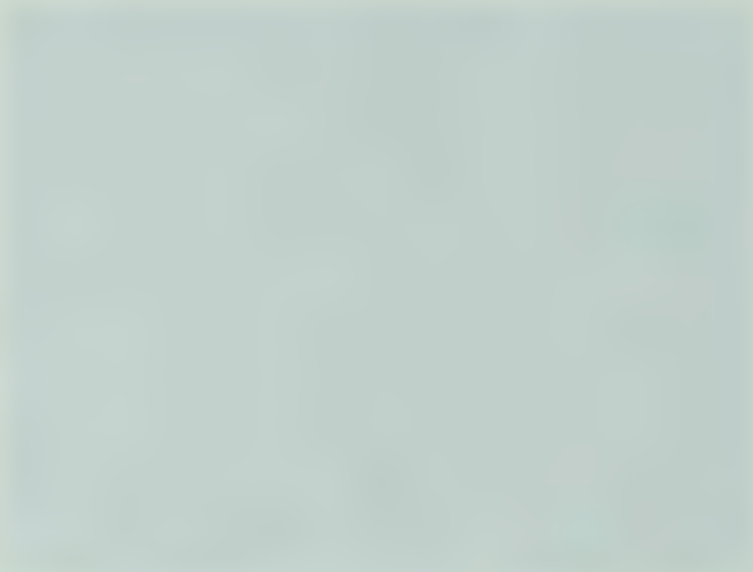


Fig. 5.4 Level detector output waveforms for different positions of integrator output.



c

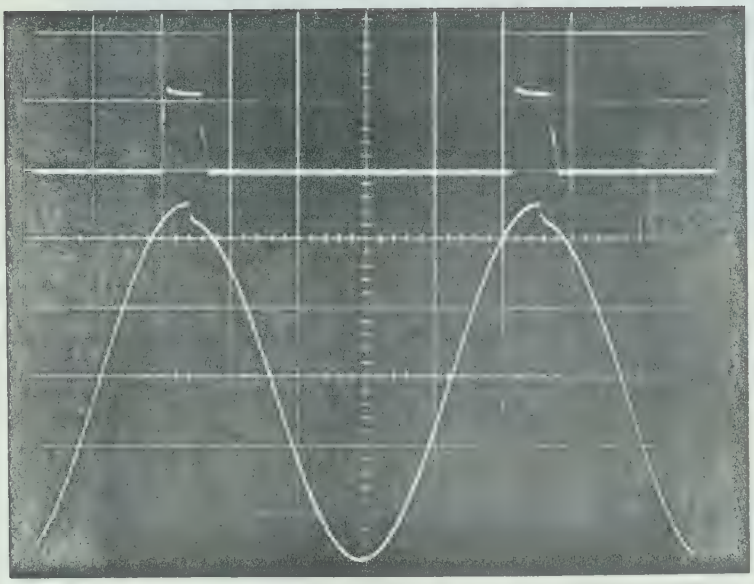


Fig. 5.4 (Continued)

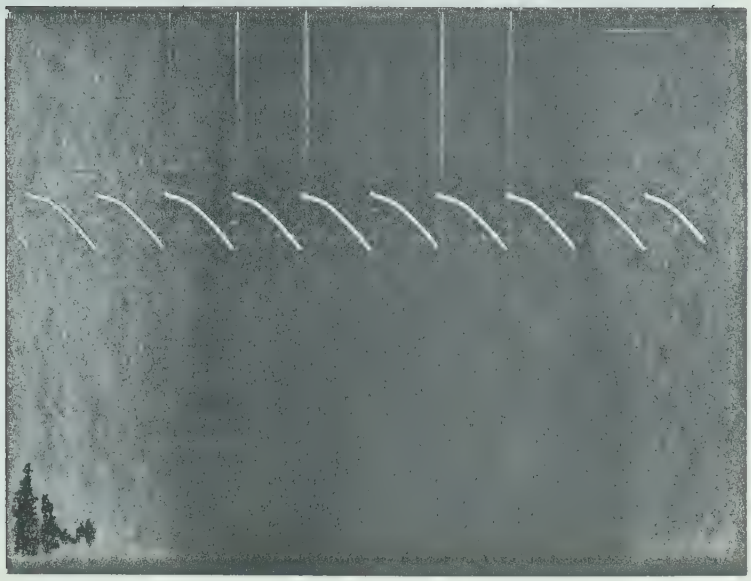


Fig. 5.5 Output D.C. voltage for α_1=30°, α_2=30°
(Test Results)

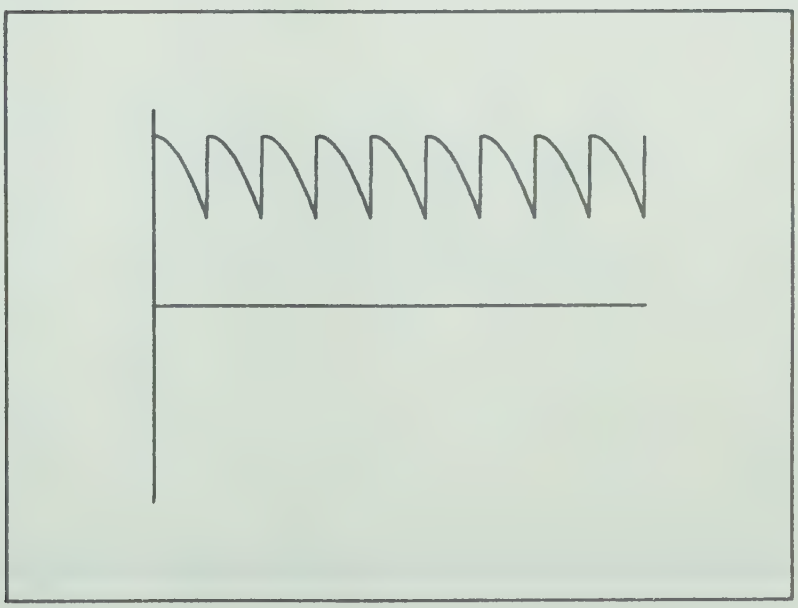


Fig. 5.12 Output D.C. voltage for α_1=30°, α_2=30°
(Theoretical Waveforms)

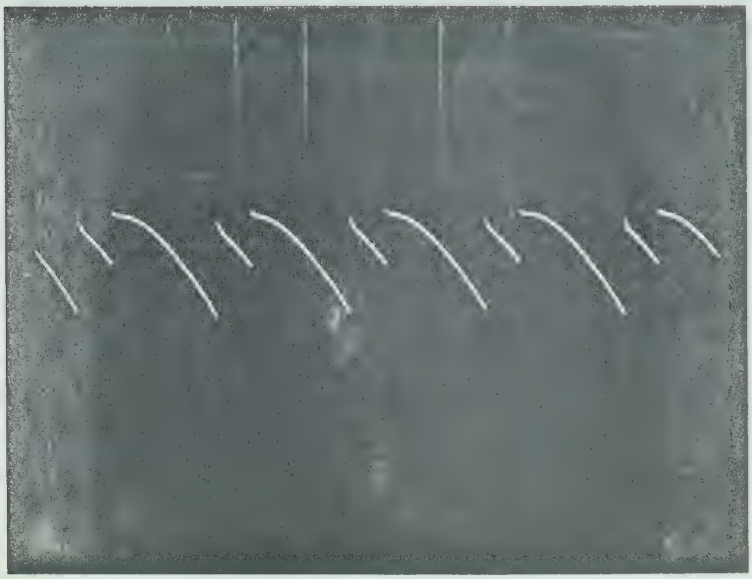


Fig. 5.6 Output D.C. voltage for α_1=60°, α_2=30°
(Test Results)

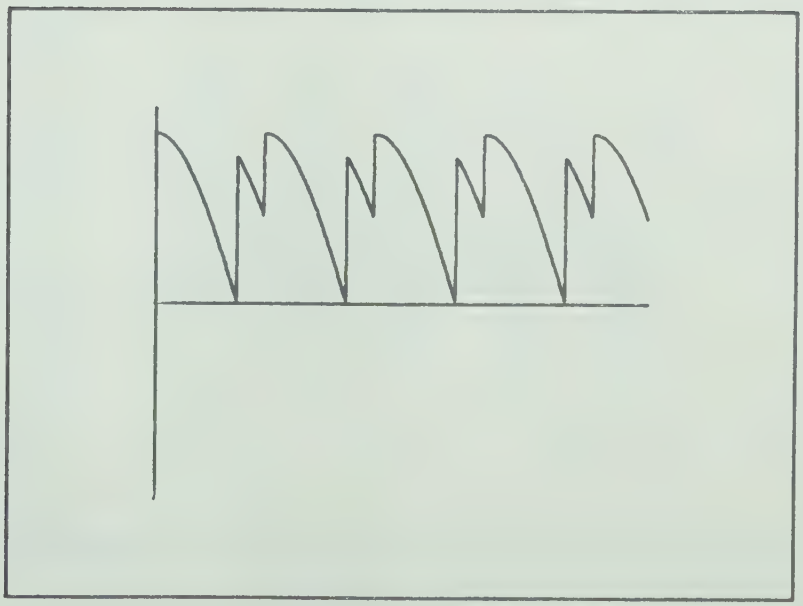


Fig. 5.13 Output D.C. voltage for α_1=60°, α_2=30°
(Theoretical Waveforms)

Fig. 5.7 Output D.C. voltage for α_1=90°, α_2=30°

(Test Results)

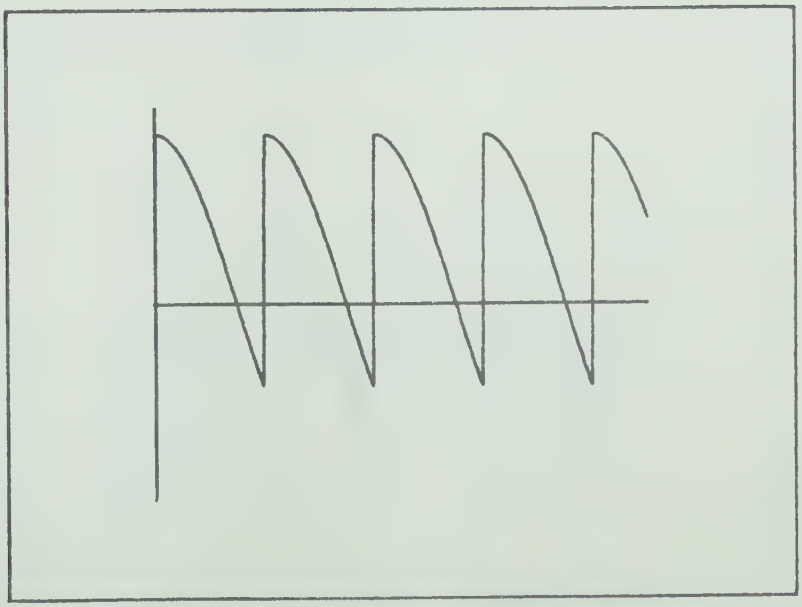


Fig. 5.14 Output D.C. voltage for α_1=90°, α_2=30°

(Theoretical Waveforms)

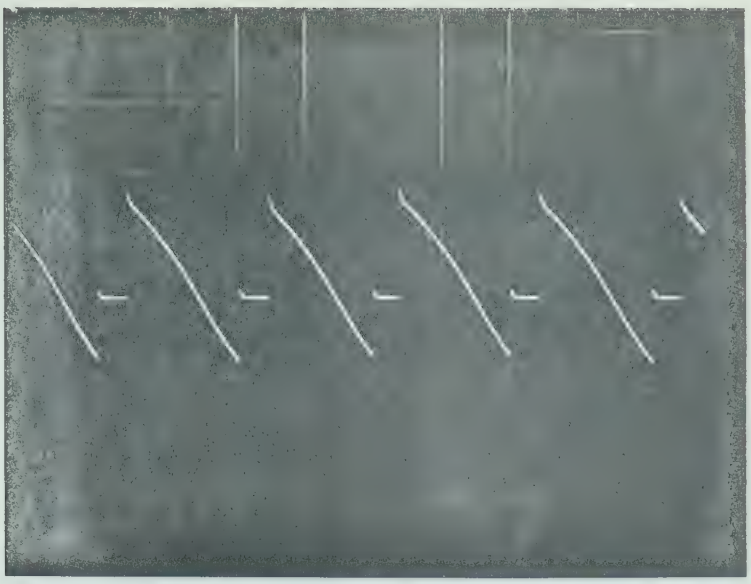


Fig. 5.8 Output D.C. voltage for α_1=120°, α_2=30°

(Test Results)

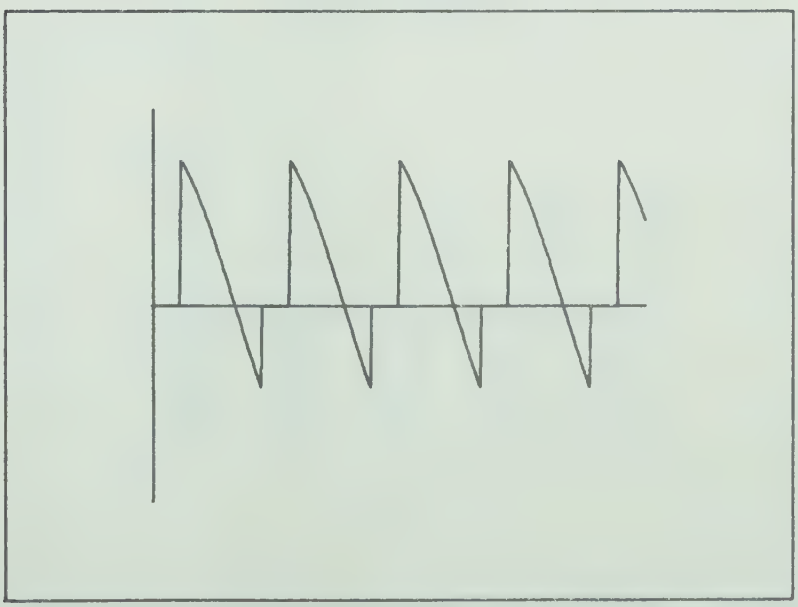


Fig. 5.15 Output D.C. voltage for α_1=120°, α_2=30°

(Theoretical Waveforms)

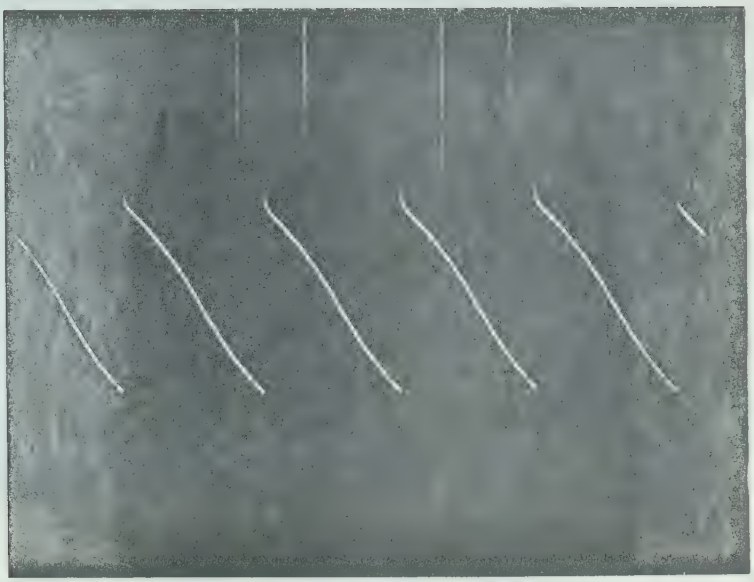


Fig. 5.9 Output D.C. voltage for α_1=120°, α_2=60°

(Test Results)

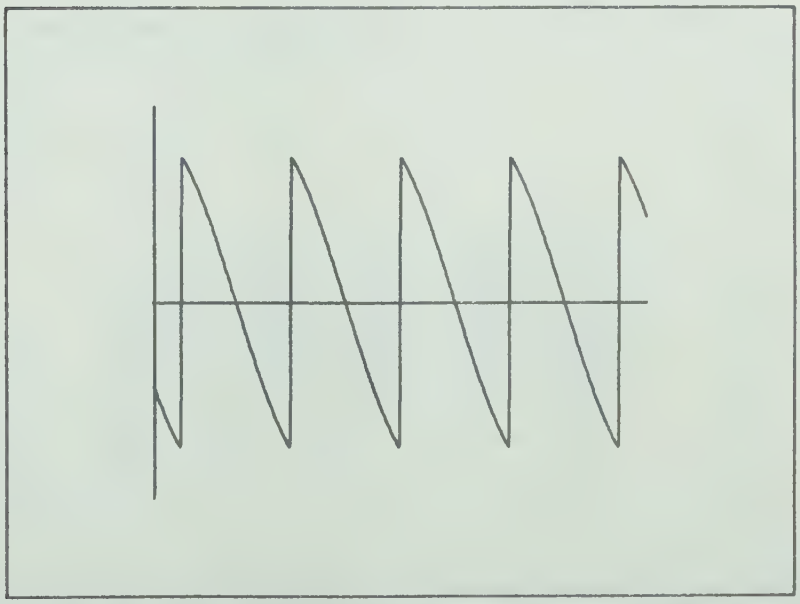


Fig. 5.16 Output D.C. voltage for α_1=120°, α_2=60°

(Theoretical Waveforms)

Fig. 5.10 Output D.C. voltage for α_1=120°, α_2=90°
(Test Results)

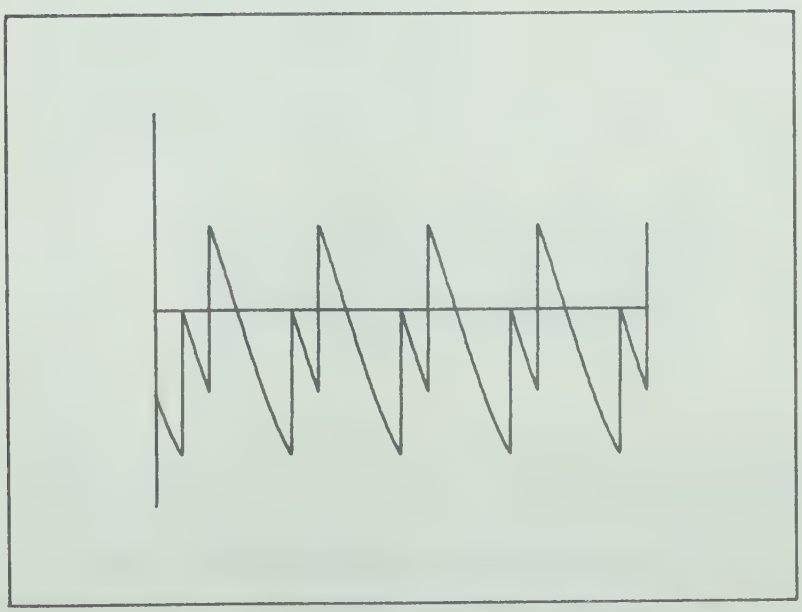


Fig. 5.17 Output D.C. voltage for α_1=120°, α_2=90°
(Theoretical Waveforms)

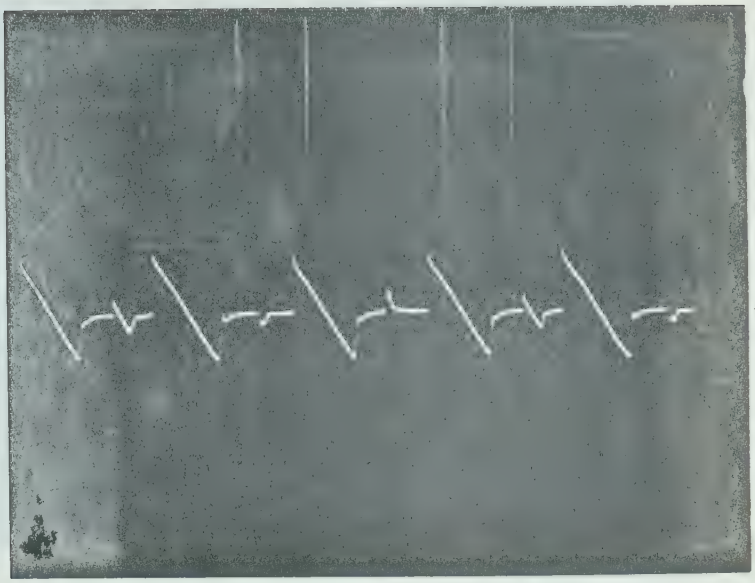


Fig. 5.11 (a) Output D.C. voltage for α_1=120°, α_2<90°

(Test Results)

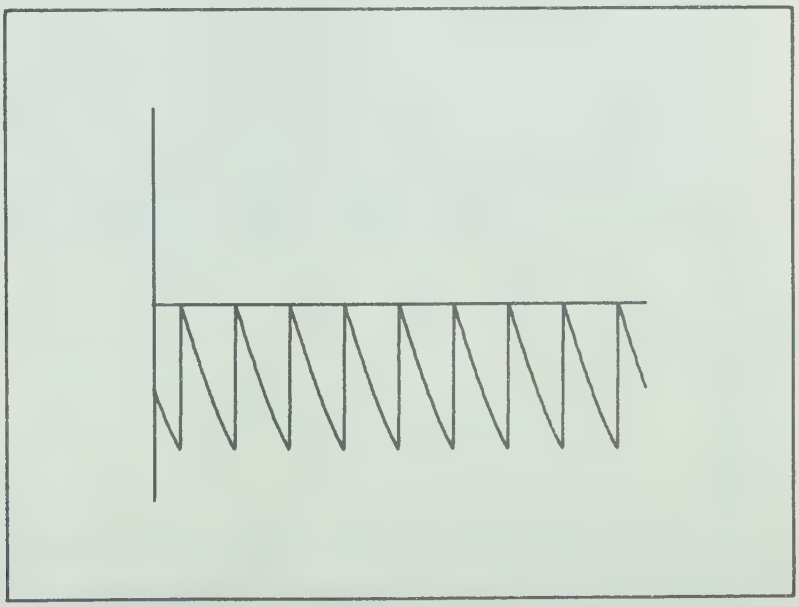


Fig. 5.18 Output D.C. voltage for α_1=120°, α_2=120°

(Theoretical Waveforms)

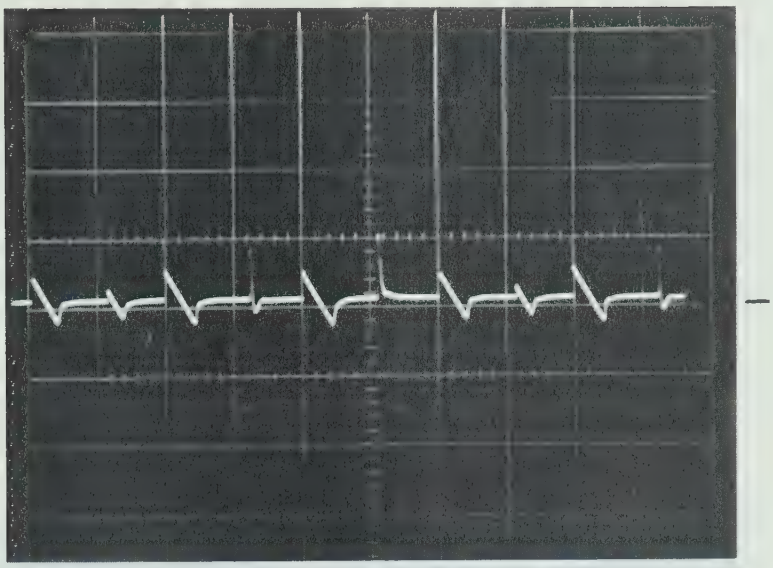


Fig. 5.11 (b) Output D.C. voltage for α_1=120°, α_2>90°

(Test Results)

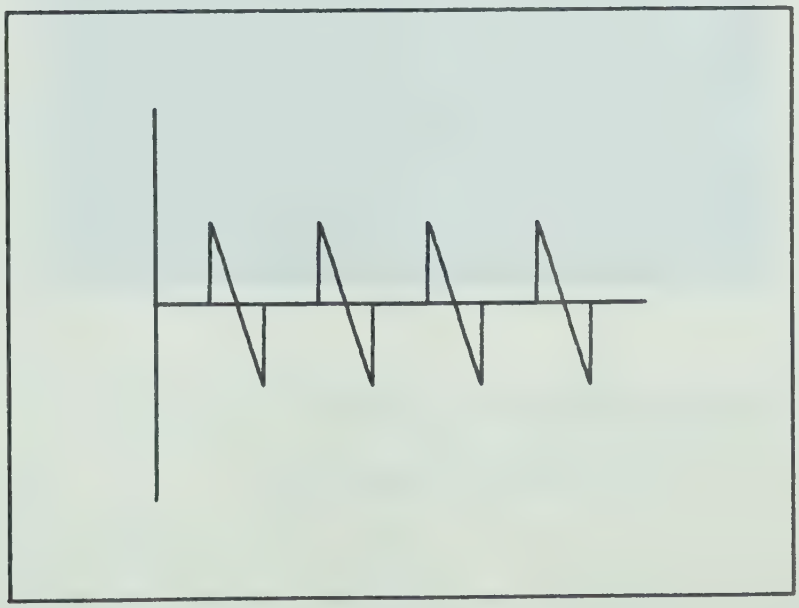


Fig. 5.19 Output D.C. voltage for α_1=150°, α_2=150°

(Theoretical Waveforms)

a

b

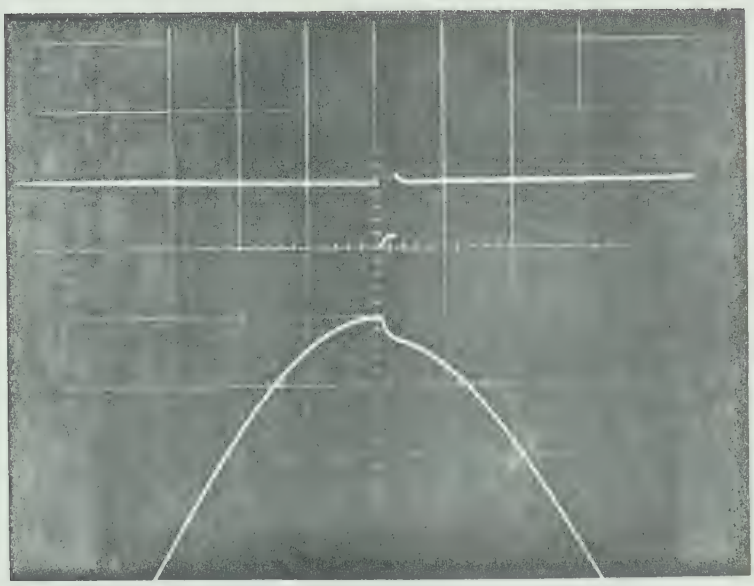


FIg. 5.20 (a) Output of monostable circuit

(b) Output of integrator

4. Although no test results were obtained in the inversion region, the control circuit performs successfully for any firing angle in the rectification region. It is believed that if the same system were tested with an active load, the performance will be the same as that obtained by the theoretical analysis.

CHAPTER VI

CONCLUSIONS

A new control system for the phase controlled converter has been presented in this work. This system has the following special features

1. The new control uses a consecutive mode of operation- in which the upper and lower groups are gated independently- and not a concurrent one as for conventional controls.

2. The control technique is based on CEA control in the inversion region. Extension of control over the whole range is done easily.

3. Control over the rectification region was done without using feedback as in conventional controls. The control signal is an external one. This makes it easy to adjust the control characteristic to any shape or form desired.

4. Linearity between the output mean d.c. voltage and the control signal is often desired. This is achieved with the new control.

5. Computation of the firing instants is freshly carried out for each cycle, and any sudden fall in a.c. voltage only affects the computation for that particular cycle.

6. The transient compensation is carried out by a simple extension to the control circuit.

7. The integration involved nearly cancels out the effect of any distortion of the a.c. voltage that might exist over the whole cycle.

8. The fundamental ripple frequency at the d.c. terminals of the converter with the new control is reduced by a factor 2:1 by using the new control.

9. By choosing the minimum value of α_2 the angle of delay for the lower valves as small as possible and the maximum value of α_1 the angle of delay for the upper valves as high as possible, the harmonic contents for zero output voltage approaches zero. Instead, in conventional controls, the zero output voltage could only be obtained at $\alpha = 90°$ at which the harmonic content reaches its maximum value.

10. In general, the harmonic contents in the output voltage using the new control are higher than that in conventional control. However, it is possible to choose the normal operating point such that the harmonic contents are as small as possible.

11. The requirements of all the components used in the control circuit could easily be achieved by using available low-cost ones.

12. The same control circuit could be used to any size of converters provided that the firing pulses are adjusted for the SCR's used.

13. While in this case the converter was intended to supply a generator field winding, the chief advantage of this method, that is, lower reactive loading of the a.c. side, is of great importance in high-voltage d.c. power transmission and many other applications of converters.

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2. J.D. Ainsworth, "The Phase-Locked Oscillator - A New Control System For Controlled Static Converters", IEEE Transactions On Power Apparatus And Systems, Vol. PAS-87, No. 3, March 1968.

3. Narain G. Hingorani and Philip Chadwick, "A New Constant Extinction Angle Control For AC/DC/AC Static Converters", IEEE Transaction On Power Apparatus And Systems, Vol. PAS-87, No. 3, March 1968.

4. Allan Ludbrook, and Robert M. Murray, "A Simplified Technique For Analyzing The 3-Phase Bridge Rectifier Circuit", IEEE Transactions on Industry And Applications, May/June 1965.

5. Narain G. Hingorani,"Single-Phase Bridge Converter With A New Control and a Corresponding Three-Phase Converter - 1. Operational Features", Direct Current, Vol. 1 (New Series) No. 1, 1969.

6. Narain G. Hingorani and Philip Chadwick,"Single-Phase Bridge Converter With a New Control and a Corresponding Three-Phase Converter - II Method of Control", Direct Current, Vol. 1 (New Series), No. 1, 1969.

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APPENDIX I

COMMUTATING EQUATION[3]

It is well known that the commutation process involves a phase-to-phase short circuit, as shown in Fig. 3.1 for commutation from 1 to 3.

If it is expected that direct current may also change during commutation, the equation for the short-circuited loop is the following:

$$\sqrt{2}\,\hat{V}_N \sin \omega t = L \frac{di_s}{dt} + \frac{Ld(i_s - i_d)}{dt}$$

$$= \frac{2Ldi_s}{dt} - \frac{Ldi_d}{dt}$$

Rearranging gives:

$$-\sqrt{2}\,\hat{V}_N \sin \omega t + 2\omega L \frac{di_s}{d\omega t} - \omega L \frac{di_d}{d\omega t} = 0$$

integration of the preceeding equation gives:

$$\sqrt{2}\,\hat{V}_N \cos \omega t + 2\omega L i_s - \omega L i_d + \text{constant} = 0$$

when $\omega t = \alpha$, $i_s = 0$ and if $i_d = I_{d_1}$

$$\text{constant} = \omega L I_{d_1} - \sqrt{2}\,\hat{V}_N \cos\alpha$$

At the end of commutation when $\omega t = \alpha + \mu$, if $i_d = I_{d_2}$ then $i_s = I_{d_2}$ and substituting in the preceeding equation gives:

$$-\sqrt{2} \times \hat{V}_N \cos\alpha + \sqrt{2}\ \hat{V}_N \cos(\alpha+\mu) + \omega L\ (I_{d_1}+I_{d_2}) = 0$$

For the corresponding equation in inverter angles, substituting $\alpha = \pi - \beta$ and $\alpha + \mu = \pi - \delta_c$,

$$\sqrt{2}\,\hat{V}_N \cos\beta - \sqrt{2}\,V_N \cos\delta_c + \omega L(I_{d_1} + I_{d_2}) = 0$$

If I_d is the average current during commutation then the last equation could be written as:

$$\sqrt{2}\,\hat{V}_N \cos\beta - \sqrt{2}\,\hat{V}_N \cos\delta_c + 2\omega L I_d = 0$$

APPENDIX II

TECHNICAL DATA FOR CONTROL

CIRCUIT COMPONENTS

No. given to component in Fig. 4.1	Name	Function	Type
1	Level detector A	To detect the zero crossing going negative of the input waveform	MC 1710 CG (Motorola)
2	Monostable circuit	To produce a pulse of width δ_c to control the FET	Fairchild 7400
3	Integrator with zero holding gate	To integrate the input sine wave, A FET is used as the holding gate	MC 1439G (Motorola) MOS P-channel FET 3N155
4	Summing Amplifier	Summation of input waveforms	MC 1439G
5	Level detector B	To detect the zero crossing going positive of the summation waveform	MC 1710CG

APPENDIX III

CHARACTERISTICS OF SCR TYPE 2N 690(10)

C35

(TYPE 2N681–2N692)
Medium Current
Silicon Controlled Rectifier
35 Amperes RMS Max.
Outline Drawing No. 5

- Broad Voltage Range—Up to 800V (440 Volt RMS Applications)
- Thermal Fatigue Free
- No Peak Forward Voltage Limitation
- Standard TO-48 Outline
- Designed to Meet MIL-S-19500/108A
- Backed by 6 Years of Design and Field Experience

Type	Minimum Forward Breakover Voltage $V_{(BR)FX}$† $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage V_{ROM} (rep)† $T_J = -65°C$ to $+125°C$	Non-repetitive Peak Reverse Voltage (<5.0 Millisec.) V_{ROM}(non-rep)† $T_J = -65°C$ to $+125°C$
C35U (2N681)	25 Volts*	25 Volts*	35 Volts*
C35F (2N682)	50 Volts*	50 Volts*	75 Volts*
C35A (2N683)	100 Volts*	100 Volts*	150 Volts*
C35G (2N684)	150 Volts*	150 Volts*	225 Volts*
C35B (2N685)	200 Volts*	200 Volts*	300 Volts*
C35H (2N686)	250 Volts*	250 Volts*	350 Volts*
C35C (2N687)	300 Volts*	300 Volts*	400 Volts*
C35D (2N688)	400 Volts*	400 Volts*	500 Volts*
C35E (2N689)	500 Volts*	500 Volts*	600 Volts*
→ C35M (2N690)	600 Volts*	600 Volts*	720 Volts*
C35S (2N691)	700 Volts*	700 Volts*	840 Volts*
C35N (2N692)	800 Volts*	800 Volts*	960 Volts*

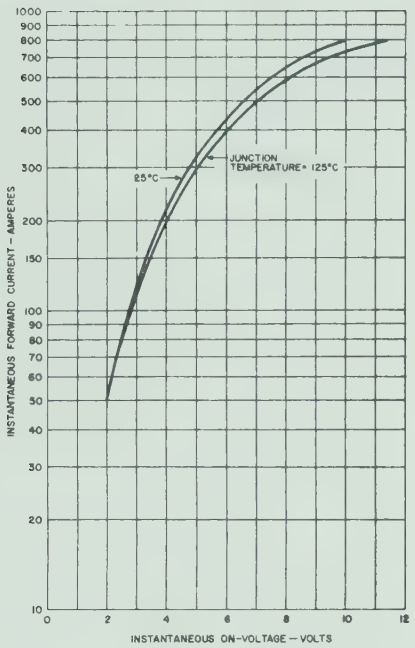
MAXIMUM ALLOWABLE RATINGS

RMS Forward Current, On-State, I_T . . . . . 35 amperes (all conduction angles)
Average Forward Current, On-State, $I_{F(AV)}$ . . . . . Depends on conduction angle (see Chart 2)
Peak One-cycle Surge Forward Current, I_{FM} (surge) . . . . . 150 amperes*
I^2t (for fusing) . . . . . 75 ampere² seconds (for times $\geq$ 1.5 milliseconds)
Peak Gate Power Dissipation, P_{GM} . . . . . 5 watts*
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 0.5 watt*
Peak Forward Gate Voltage, V_{GFM} . . . . . 10 volts*
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 volts*
Storage Temperature, T_{stg} . . . . . −65°C to +150°C*
Operating Junction Temperature, T_J . . . . . −65°C to +125°C*
Stud Torque . . . . . 30 inch-pounds
Peak Non-Recurrent Surge Forward Current During Turn-on Time Interval . . . . . See Chart 6

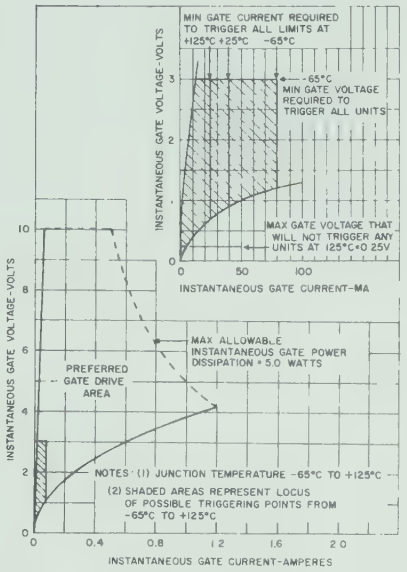
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Gate Trigger Current	I_{GT}		15	40	mAdc	$T_J = 25°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
			35	80*	mAdc	$T_J = -65°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
			10	25	mAdc	$T_J = 125°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
Gate Trigger Voltage	V_{GT}	....	1.5	3.0*	Vdc	$T_J = -65°C$ to $125°C$, $V_{FX} = 6$ Vdc, $R_L = 50$ ohms
		0.25*			Vdc	$T_J = 125°C$, V_{FXM} = Rated, $R_L = 1000$ ohms
Holding Current	I_{HO}	....	10	100	mAdc	$T_J = 25°C$, Anode supply = 6 Vdc
Turn-on Time (Delay Time + Rise Time)	$t_d + t_r$	....	1.4	....	μsec.	$T_J = 25°C$, $I_F = 5$ Adc, V_{FXM} = rated. Gate supply: 10 volt open circuit, 25 ohm, 0.1 μsec. max. rise time.
Circuit-Commutated Turn-off Time	t_{off}		20		μsec.	$T_J = 125°C$, $I_{FM} = 10A$, I_R (recovery) = 5A, V_{FXM} (reapplied) = Rated. Rate of rise of reapplied Forward Blocking Voltage = 20 volts/μsec. linear.
Effective Thermal Resistance	θ_{J-C}	. .	0.85	1.7	°C/watt	Junction to Case.
Exponential Rate of Rise of Forward Blocking Voltage	τ				μsec.	$T_J = 125°C$. Gate open circuited. V_{FOM} = Rated.
C35U (2N681)		2.6	....	....		
C35F (2N682)		3.0				
C35A (2N683)		3.9	.	.		
C35G (2N684)		4.8				
C35B (2N685)		5.7	.	.		
C35H (2N686)		6.6	. .			
C35C (2N687)		7.5				
C35D (2N688)		9.2				
C35E (2N689)		11.0		.		
→ C35M (2N690)		37.9				
C35S (2N691)		44.2				
C35N (2N692)		50.6				

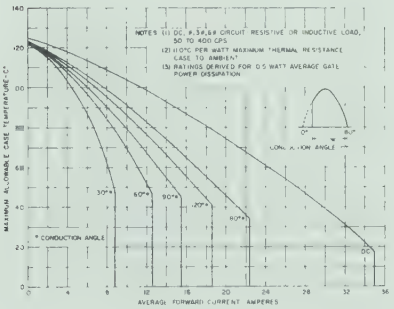
† Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 11°C/watt.
* Indicates data included on JEDEC type number registration.



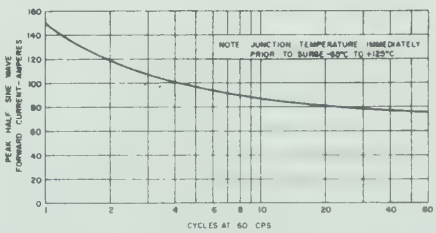
1. Maximum Forward Characteristics—High Current Level—On-State



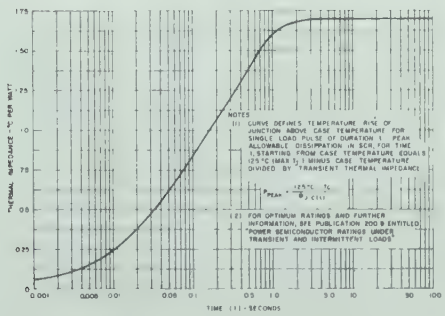
3. Gate Triggering Characteristics



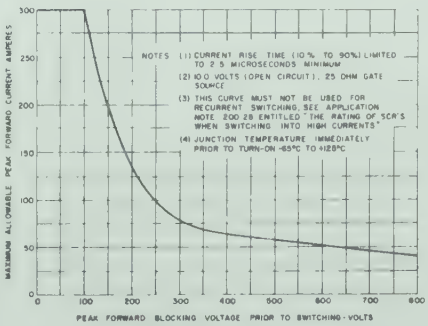
2. Maximum Allowable Case Temperature For Sinusoidal Current Waveform



4. Maximum Allowable Non-Recurrent Peak Surge Forward Current at Rated Load Conditions



5. Maximum Transient Thermal Impedance —Junction to Case



6. Peak Non-Recurrent Surge Forward Current During Turn-On Time Interval